9950-203

DOE/JPL 954847-78/4
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PHASE 2 OF THE AUTOMATED ARRAY ASSEMBLY TASK

OF THE LOW-COST SILICON SOLAR ARRAY PROJECT

(NASA-CR-162429) THE AUTOMATED ARRAY ASSEMBLY TASK OF THE LOW-COST SILICON SOLAR ARRAY PROJECT, PHASE 2 Annual Report (Motorola, Inc.) 213 p HC A10/MF A01 CSCL 10A G3/44

N80-11562

Unclas 46085

NOVEMBER 1978

JPL CONTRACT NO. 954847

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THE JPL LOW-COST SOLAR ARRAY PROJECT IS SPONSORED BY THE U. S. DEPARTMENT OF ENERGY AND FORMS PART OF THE SOLAR PHOTOVOLTAIC CONVERSION PROGRAM TO INITIATE A MAJOR EFFORT TOWARD THE DEVELOPMENT OF THE LOW-COST SOLAR ARRAYS. THIS WORK WAS PERFORMED FOR THE JET PROPULSION LABORATORY, CALIFORNIA INSTITUTE OF TECHNOLOGY BY AGREEMENT BETWEEN NASA AND DOE.

PROJECT NO. 2345

DOE/JPL 954847-78/4
DISTRIBUTION CATEGORY UC-63

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ANNUAL REPORT

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1.0 SUMMARY

This report presents the results of investigations and analyses of an advanced process sequence for manufacturing high efficiency solar cells and modules in a cost-effective manner. The entire process sequence is presented and discussed step by step. Emphasis is on process simplicity and minimizing consumed materials. The process sequence incorporates texture etching, plasma processes for damage removal and patterning, ion implantation, low pressure silicon nitride deposition, and plated metal. A reliable module design is presented. Specific process step developments are presented. Further, a detailed cost analysis has been performed to indicate future areas of fruitful cost reduction effort. Finally, recommendations for advanced investigations are presented.

2.0 INTRODUCTION

There is a high probability that flat plate solar photovoltaic modules will become a major source of electricity generation throughout most of the world, and that the silicon solar cell will be the preferred generating element. In order to provide a realistic framework on which to build an effective program of R&D and demonstration for silicon solar cell modules, a series of objectives has been established which lead to a 1987 goal of 50¢ per peak watt. At this price, solar-generated electricity will be able to compete with electric power generated by any other means, provided the solar cell modules are sufficiently reliable (e.g., have a mean life of over 20 years).

To reach the 1986 JPL goal will require several advancements: 1) a cheaper source of pure silicon, 2) a much more economical way of transforming the source silicon into large, thin, (essentially) single crystal substrates having a controlled geometry, 3) an economical, large module package that will protect the interconnected solar cells it contains for at least 20 years from degradation caused by exposure to the weather, 4) an automated process sequence that produces high efficiency, reliable, cheap solar cells, tests them, interconnects them, and encapsulates them, and 5) a large market, of the order of 500 Mw/year.

When the JPL/ERDA Project started, the Motorola Solar Energy R&D Department participated in Phase I of The Automated Array Assembly Task. The Phase I study identified a few potentially powerful process sequences for silicon solar cell production, and experimentally verified the overall consistency of the process sequence. It concluded that no basic technological innovations were necessary for solar cell fabrication or encapsulation in

order to meet the long range Project goals. Detailed economic analyses were performed, based on today's technologies, and showed that it would be possible to meet the JPL cost projections for solar panels.

The overall conclusion of the Array Automated Assembly Task, Phase I, was one of cautious optimism. The present program, for Phase 2, had as its objective the further development of specific process steps (in a specified, powerful process sequence) leading to a completely specified solar cell (and module) production process sequence. This sequence is capable of a high degree of automation and control. A detailed economic analysis was a major part of the program to ensure that the approach taken was cost-effective.

3.0 TECHNICAL DISCUSSION

An advanced process sequence for manufacturing silicon solar cell modules has been specified; it is ready for development into production readiness. This process is expected to be capable of producing cells with the highest cost-effective efficiency possible from any given quality of starting material. It has been concluded that maximum cost-effectiveness is enhanced when a minimum of materials is consumed in the process sequence. As a result, emphasis has been placed on the minimization of consumed materials during the development of this process sequence. The two factors, high cell efficiency and minimization of consumed materials, are consistent with the third goal of high process yields achieved through well-defined process controls. The true cost effectiveness of any product is reflected in its serviceable life, not just in its initial cost. Accordingly, attention has also concentrated on the reliability of the product manufactured by this process sequence. The goal is to optimize cost effectiveness through maximization of module operating life.

3.1 THE PROCESS SEQUENCE

The specific process sequence is outlined below:

1. Etch starting material
   a. Cz to remove saw damage
   b. Sheet, as-grown, to remove surface layer*
2. Apply etch stop - one side
3. Texture etch and remove etch stop
4. Ion implant back surface field region (high-low junction)
5. Ion implant front p-n junction
6. Activation anneal of implant**

7. Chemical vapor deposition of silicon nitride**
8. Form metallization pattern in silicon nitride
9. Plate metal and solder coat
10. Cell test and solder reflow interconnect
11. Encapsulate

* This may not be necessary with sheet produced by some processes.

**These steps may be done concurrently

The rationale and description of each of the process steps, and interactions within the process sequence, are presented in this section.

3.1.1 STEP ONE: ETCH STARTING MATERIAL

The input material for this process sequence is assumed to be either 1) sliced Cz material, obtained in the as-sawed condition, or 2) a form of continuously grown silicon sheet material. In either case, the first step in the process sequence will be an etch to remove the surface layer of silicon.

For the case of as-sawed Cz material, the sawing operation leaves a heavily damaged surface layer. This layer contains microscopic cracks and slipped regions of silicon as a result of the sawing operation. Silicon particles torn away from one region may be mechanically forced into other regions, producing an effect similar to smearing. Material worn from the saw itself, slurry particles, and/or other foreign material (e.g., contaminants) may be forcefully lodged into the silicon surface. Surface damage can propagate deeply into the silicon during subsequent high temperature processing, degrading crystalline perfection and reducing minority carrier lifetime. Also, contaminants trapped in the fine interstices of a damaged surface may diffuse into the silicon

during such high temperature processing steps, degrading lifetime as well. Below the heavily damaged surface layer is found a more lightly damaged layer, containing slip and strain, which can contribute to the formation of dislocations and dislocation networks upon heating. Such damage sites may act as recombination centers and also have an adverse effect upon minority carrier lifetimes. Further, such damage may be interactive with processing steps of junction formation in a non-uniform and uncontrollable manner. Accordingly, major damage from sawing must be removed in order to achieve satisfactory process control, and yield of solar cells with uniform cell efficiency.

Continuously grown silicon sheet material, such as is grown by the edge-defined film-fed growth (EFG) technique or by the ribbon-to-ribbon (RTR) technique, may also require surface etching. Reports, both formal and informal, by several companies with major programs in this area, have indicated that improved solar cell efficiencies were obtained on EFG material which had been surface etched rather than utilized in the as-grown condition. The improvement of solar cell efficiency utilizing EFG ribbon following removal of the surface layer has been postulated to be a result of placing the p-n junction in a region containing a dramatically lower concentration of either oxygen or carbon (or both) than exists in the as-grown surface layer. If the cause is, in fact, removal of an oxygen-rich layer from the surface, any as-grown sheet material may be improved by surface etching. Although evidence from EFG technology indicates that a surface-etching step is desirable for as-grown silicon sheet material, it is not known whether all (or indeed any) of the silicon sheet-growth techniques under investigation need to have such a surface layer removal. If silicon sheet with good surfaces is achieved in the future, then this first step can be eliminated from the process sequence.

A smooth surface on the silicon material after etching is desired for all material in order that the back surface of a solar cell be flat and thus allow utilization of back surface total internal reflection.

Surface etching of silicon can be achieved by wet chemical techniques. Wet chemistry etching is a proven technology that is widely utilized in the semiconductor industry. Wet chemistry, however, consumes volumes of materials such as bases or acids and deionized (DI) water, and thus is inherently limited in cost to the price of these consumed materials. Further, a disposal problem exists for waste acids or bases, adding to the cost of wet chemistry etching.

An alternative to wet chemical etching is plasma etching of the silicon surface. In plasma etching technology, the silicon is placed in a reduced pressure chamber filled with low partial pressures of gases such as CF_4 and O_2. The CF_4 and O_2 are ionized with an RF field, forming an energetic plasma of ionized fluorine and oxygen which will attack and etch silicon. Reaction products follow the gas stream and are swept from the reaction chamber, allowing continuous etching to occur. Consumed materials costs, and waste disposal problems, are minimal compared to wet chemistry etching.

The first step in the solar cell process sequence, thus, incorporates plasma technology for etching the starting silicon material. If a technique for growing silicon ribbon with high surface quality is developed, this step may be eliminated.

3.1.2 STEP TWO: APPLY ETCH STOP

Following the formation of smooth surfaces from the first step (silicon etching), one side of the silicon is texture etched while maintaining the smooth

surface on the opposite side of the substrate. In order to achieve this, one side of the silicon must be masked against the texture etchant. A wax resist technology has been specified for this process step.

Masking of one side of a silicon sheet can be accomplished by a variety of ways, including application of tape; photoresist spinning or spraying; and spinning or spraying other types of resists. Since masking of one side for texture etching requires only blanket coverage, a very simple surface covering technique may be used. Such a masking operation could result in consumption of materials that do not appear in the final solar cell; to minimize costs of materials, energy usage, and waste disposal, it would be desirable to utilize a recyclable masking material. As a result, Motorola investigated the use of a wax resist. The wax may be dissolved in a solvent, sprayed upon one side of the silicon, and the solvent evaporated from the wax, leaving a wax coating upon one side of the silicon. The evaporated solvent would be reclaimed, at least in part, by condensation. The wax could then be subsequently removed in the solvent. Both the wax and solvent can, thus, be continually recycled, reducing consumed materials to a very small level. Alternatively, the wax can be applied in a molten form without the use of solvents, and removal can be achieved by floating off in a heated bath.

3.1.3 STEP THREE: TEXTURE ETCH AND REMOVE ETCH STOP

The silicon is next texture etched on one side. Texturing is an anisotropic etching process, which has been developed to the point where it is now a simple, well-developed, and controllable step. The process incorporates a simple bath-etching technique which requires minimal capital investment.

Texture etching of (100) Cz wafers is a proven technology and has been incorporated in production process sequences at Motorola to produce high efficiency solar cells.

As-grown silicon sheet material may be oriented with surfaces other than (100). If the silicon sheet is (large grain) polycrystalline, several crystallographic orientations will be present. Accordingly texture etching will produce different results on these different orientations. If as-grown sheet can be seeded to grow (100) surfaces, processing should be identified to that developed for (100) Cz wafers. Some as-grown sheet has been shown to have a structure of (100) surfaces and <112> axial orientation; texturing of such surfaces has been reported.

Over the next several years, each promising silicon sheet growth technique will be investigated with respect to its capabilities for producing material with a specific surface orientation. It is assumed here that sufficient orientation control will be obtained so that some texture etching can be performed effectively. If this proves not to be the case, then either sheet-grown silicon will suffer an inherent disadvantage, or effective texturing techniques must be found for the grain orientations found on sheet-grown silicon surfaces.

Following texture etching, the wax resist is removed by dissolution in the original solvent carrier or floated off in a heated bath, as discussed in Section 3.1.2.

To ensure that all wax and solvent residue are removed from the silicon surfaces, the silicon must be cleaned further. Two choices are possible: 1) wet chemistry cleaning or 2) plasma cleaning. Again, plasma cleaning is preferred. This cleaning is performed in an oxygen-rich plasma (air is adequate) and is identical to a process widely utilized throughout the semiconductor industry to remove photoresist. (The accepted terminology for an oxygen plasma removal of films which are primarily organic is "ashing".)

3.1.4 STEPS FOUR AND FIVE: ION IMPLANTATION OF FRONT AND BACK JUNCTIONS

Dopants for forming the metallurgical p-n junction in the textured front surface and the back surface field high-low junction in the smooth back surface are ion implanted into the silicon. There is broad industrial agreement that junction formation in future solar cells will be done by ion implantation, assuming that advanced reliable ion implantation equipment will be developed to supply sufficiently high ion beam currents to allow increased throughput over today's existing equipment.* Such advanced equipment appears completely feasible, based on projections of ion implanter manufacturers.

Ion implantation of the dopants may be performed directly into the bare silicon surface or following deposition and patterning of the silicon nitride layer. Each alternative has its own advantages; the choice will be made on cost effectiveness.

When ion implantation is done into a bare silicon surface, the distribution of implanted ions is dependent upon the energy of the incident ions, and is Gaussian in nature. Increased ion energy will move the peak concentration of the distribution further beneath the surface. The actual distribution of as-implanted dopants is skewed deeper into the silicon due to an effect known as channelling. Ions implanted along the major crystallographic directions in a crystalline material will penetrate much further than those implanted in other crystallographic directions, since the major directions are more open to ions, i.e., present channels for the ions.

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*This does not mean that the ion beams must be of high current density. It would be better, in fact, to have a rather diffuse beam of high total ion current.

In an alternative to this process sequence, the front surface dopant used to form the p-n junction may be implanted through a silicon nitride layer under conditions such that the peak as-implanted dopant concentration is very near the dielectric-silicon interface. (The stopping powers of silicon nitride and silicon are similar, but not equal.) This requires a relatively high ion energy to penetrate the nitride layer. If the peak concentration of the distribution occurs at the dielectric-silicon interface, approximately one-half is in the dielectric. Having the peak dopant concentration at the silicon surface is desirable in that the doping decreases monotonically towards the p-n junction, creating an electric field away from the surface and thus aiding in carrier collection at the p-n junciton. Further, the silicon nitride surface layer, being amorphous, acts as a moderator and scattering medium for implanting ions, minimizing channelling effects and maintaining a uniform shallower junction profile.

If the silicon nitride layer is patterned with the metallization contact pattern prior to ion implantation, these openings are ion implanted under different conditions than the areas under the silicon nitride. First, since there is no silicon nitride to absorb ions, dopant concentration in the exposed silicon is approximately twice that in the dielectric-covered regions, and the peak concentration is deeper than in the dielectric-covered regions. Second, since there is no dielectric layer to cause scattering, some further penetration due to channelling can be expected. Following implant activation (discussed in Section 3.1.7) the p-n junction beneath the openings in the silicon nitride is deeper than the p-n junction under the silicon nitride. This additional junction depth under the metal contact can be desirable to allow formation of strongly adherent contacts by reaction with the silicon without penetration to (and thus degradation of) the p-n junction by the metal.

The advantages of implanting through a silicon nitride layer having been patterned with the ohmic contact pattern have been discussed. The primary disadvantages to this alternative are the high energy required to penetrate through the silicon nitride and the utilization of only about half of the total ion beam does in the silicon, the remainder being trapped within the silicon nitride layer.

While implantation through a dielectric such as silicon nitride has advantages, it presently appears that implanting into a bare surface is more cost effective. First, cell throughput can be approximately doubled by utilizing all of the implanted dose directly in the silicon. In order to retain both the desired shallow junction depth and the desired dopant profile away from the surface, much lower ion energies are utilized for bare surface implants than for those required to penetrate a dielectric surface layer. Accordingly, the voltage isolation requirements for (and within) the ion implanter are reduced for bare surface implantation. Logically, this should reduce design requirements for future high beam current implanters, making them both cheaper and more reliable.

Two additional features of the process sequence favor bare surface implants. First, use of the plated metallization, which has Pd_2Si as the silicon contact layer, has limited penetration into the silicon. This reduces the benefits of having a deeper p-n junction under the metal contacts. Second, and perhaps more important, implanting into a bare surface can result in a major process simplification: a combination of the activation anneal and silicon nitride deposition steps.

Ion implantation, being a directional doping process (as compared to isotropic doping from a diffusion source) has a unique advantage when applied to textured surfaces. If the ion beam is normal to the plane of the wafer, the beam will be at a large angle to the surfaces of the (microscopic) textured pyramids. The range of an ion into silicon is defined as the (average) linear thickness of silicon through which it passes before coming to rest. Since the ion beam enters a textured silicon surface at an angle to the planes of the pyramid surfaces it stays closer to the actual silicon surface than its penetration depth (even allowing for the scattering effects of a silicon nitride layer, if one is used). The resulting junction depth, as measured perpendicular to the faces of the pyramids comprising the textured surface, is less than would be seen for implantation into a plane surface.

Ion implantation into the back surface of a solar cell to form the back surface field has features similar to those characterizing implantation into the front surface. In this case, however, the surface is smooth. Implantation may be performed at a different acceleration voltage since a different doping species is being used and since the implant beam incidence is normal to the smooth surface, rather than at a large angle such as for textured pyramids. However, if implantation is performed into bare surfaces, the acceleration voltage for p-n junction and back surface field regions may be the same, simplifying the equipment and thus reducing cost.

The ion implantation process can be readily used to give a planar passivated p-n junction. If the ion beam is mechanically masked for front surface implantation, a planar p-n junction will automatically result.

An excellent p-n junction can be achieved even by implanting completely to the edge of the silicon (i.e., no physical masking).

Since the ion beam is collimated, it is virtually impossible to obtain a region implanted from both the front and back directions such that an n+ - p+ junction is formed. The need for peripheral etching is, thus, not present. Hence, ion implantation can, in a simple way, allow utilization of the entire silicon front surface for the solar cell p-n junction.

3.1.5 STEP SIX: CHEMICAL VAPOR DEPOSITION (CVD) OF SILICON NITRIDE

A layer of silicon nitride is deposited on both sides of the silicon sheet simultaneously. This is accomplished in an isothermal chamber at a pressure of less than one atmosphere, and constitutes a well-developed process. Film parameters, such as thickness and index of refraction, are highly reproducible and readily controlled.

The silicon nitride layer is an excellent example of process synergism, serving several functions in the process sequence and in the final cell. The silicon nitride serves as a plating mask during metallization, and acts as a passivant over the p-n junction. The silicon nitride layer covering the back surface can, if patterned, serve as a convenient means for providing a reflecting back surface by masking metal deposition. (As has been shown experimentally, palladium silicide, nickel silicide, and perhaps other contacts, if they form ohmic contact to silicon, are light absorbing. Masking the back from metal deposition, thus, leaves a well defined silicon surface for reflection. Total internal reflection will occur due to the large angle of incidence at the back surface resulting from refraction at the textured front surface.) Finally, and most important, after serving its process-facilitating role, the silicon nitride layer on the front surface acts as the antireflection coating over the completed cell surface. If the nitride is deposited prior to implantation,

the silicon nitride layer can act as a partial ion implantation mask to tailor concentration profiles, and, being amorphous, scatters the ion beam to reduce ion channelling effects.

Silicon nitride has an index of refraction near 2.0. While this value is lower than optimum for plane front surface cells, it performs as an excellent antireflection coating on textured surfaces. Further, silicon nitride is the best known p-n junction passivant in the semiconductor industry and as a result is widely used in silicon device and integrated circuit production. Silicon nitride has proven particularly beneficial as a passivating layer for silicon devices and integrated circuits that are encapsulated in non-hermetic (e.g., plastic) packages; in such cases the silicon component is in a package environment that approximates the one in which silicon solar cells appear.

3.1.6 STEP SEVEN: FORMATION OF METALLIZATION PATTERN IN SILICON NITRIDE

The next step in the process sequence is to pattern the silicon nitride layers on both front and back surfaces of the silicon substrate with the desired metallization pattern. This process step has historically been performed by photolithographic techniques. Under this contract, a novel plasma technique has been studied.

Photolithographic techniques and equipment are now available for sequentially coating photoresist on both sides of a silicon sheet, simultaneously exposing a pattern on both sides of the sheet, and developing these patterns to allow selective etching of the nitride. Photoresist is, however, an expensive consumable material which requires not only the steps mentioned above, but also the steps of removing the hard resist, cleaning the silicon after the dielectric pattern has been etched, and waste disposal.

Plasma etching can be utilized to etch silicon nitride. Masking to achieve selective pattern etching can be done through the use of photoresist, but the undesirable features discussed above are still fully applicable.

Gases used in plasma etching of silicon nitride do not attack some metals, such as aluminum or steel. Further, a metal mask in contact with, or in close proximity to, a silicon wafer will, in some electrode configurations, mask plasma etching behind it. A metal mask, containing the desired cell metallization pattern, thus, may be mechanically placed over the wafer, and the desired pattern formed in the silicon nitride by exposure to the appropriate plasma. The wafer can, in fact, be placed between two such masks, and patterns simultaneously formed in the silicon nitride by plasma etching on both sides of the wafer. Only the etchant gas is consumed, a tremendous advantage in materials usage over photolithography.

3.1.7 STEP EIGHT: ACTIVATION ANNEAL OF IMPLANT

Following ion implantations, the silicon lattice is heavily damaged and the implanted dopant ions are, for the most part, electrically inactive. An annealing step must be performed in order to both repair the silicon damage and to electrically activate the dopant ions. Annealing can be performed in a standard resistance-heated furnace. This technique is a proven technology employed effectively throughout the semiconductor industry, and has been utilized in solar cell fabrication. Studies performed on this contract have shown that it is possible to combine this step with the silicon nitride deposition step.

3.1.8 STEP NINE: PLATE METAL AND SOLDER COAT

Under contract DOE/JPL/954689 the use of a plated metallization system in which palladium silicide, Pd_2Si, is the electrical and mechanical contact to the silicon, has been developed. The palladium silicide is covered with electroless nickel to form a solderable surface which, at the same time, is strongly adherent to the palladium silicide. Finally, the nickel layer is solder coated

to achieve both the desired metallization conductivity and a soldered surface for subsequent reflow during interconnection. Developments under the parallel contract have been incorporated into this program.

This metallization system has proven feasibility and is currently being utilized as metallization on cells in commercially available modules.

It is expected that this metallization system will prove to be extremely reliable in terrestrial service. Palladium silicide has been used in place of platinum silicide as part of the silicon integrated circuit (and device) beam-lead metallization system in order to simplify processing for that system. (The beam-lead metallization system is considered the most reliable of all for "hi-rel" system applications.) Palladium silicide contacts are, by themselves, moisture resistant. For example, there is no observable change in any property after a long boil in deionized water. The resistance of these contacts to corrosive ambients and electrochemical reactions in service, (i.e., with nickel cap and solder overcoat), while not yet thoroughly tested, appears very optimistic.

Palladium and nickel metallization layers are deposited from plating baths. A first , an extremely thin layer of palladium is plated from an immersion bath, covering exposed silicon surfaces only; plating does not occur on the silicon nitride. The palladium layer is heat treated to form a very thin layer of Pd_2Si (which may not be completely continuous). This thin Pd_2Si layer, formed by heat treatment of the immersion plating, serves to activate the plated areas so that subsequent plating will occur in a uniform and controllable manner. A second plating of palladium from an electroless palladium bath is then formed over the Pd_2Si. This layer is thicker than that deposited from the immersion bath. The new layer is now reacted to form a continuous layer of Pd_2Si in the desired contact areas.

Several features of the Pd_2Si layer must be noted at this time. First, when Pd_2Si is formed, it is produced primarily by the solid state diffusion of silicon

into the palladium layer, with little or no palladium diffusing into silicon ahead of the Pd_2Si - Si interface. Metallic palladium ions, thus, are limited to approximately the region of the Pd_2Si. This allows the formation of Pd_2Si over very shallow p-n junctions without degradation of the p-n junction characteristics. Second, Pd_2Si has low contact resistance and excellent mechanical adherence to silicon. In addition, the Pd_2Si layer should act as a physical barrier to the migration of other metallic impurities into the p-n junction area. Since a nickel layer is utilized for soldering, this barrier feature is highly important for the very shallow p-n junctions that are utilized in high efficiency solar cells. Following the second sinter to form Pd_2Si, the cell metallization areas are plated with electroless nickel. This layer has excellent adherence to Pd_2Si and is easily solderable. The entire solar cell is then solder dipped to coat all metallization areas with a thick layer of solder.

The metallization process utilizes only chemical hoods and plating baths for the formation of metal contacts on both sides of the wafer simultaneously. The bulk of the metal conductors is composed of solder, which is relatively inexpensive compared to other conductor metals for solar cells.

3.1.9 STEP TEN: CELL TEST AND SOLDER REFLOW INTERCONNECT

Following solder coating, the solar cells are tested and interconnected. Motorola has developed a flexible circuit interconnection scheme utilizing a laminated conductor and insulating dielectric sheet; presently utilized are laminated copper and kapton. The copper can be patterned to incorporate any series, parallel, or series-parallel cell interconnection scheme desired. Tabs are cut in the laminate for contact to the top surface of the solar cell in such a manner as to obtain multiple contacts to each cell and to insure minimum stress upon the interconnection. The back cell contact is a direct solder contact from the cell back surface metallization to the copper layer. All contacts are made simultaneously by solder reflow, minimizing labor content in interconnection.

Future modules will incorporate large square or rectangular solar cells rather than round cells. Accordingiy, cell interconnection will occur either continuously or at many points along the edges of the cell, not at isolated points as now utilized in round cells. This feature will dramatically change the interconnect structure from that presently utilized. It is envisioned that individual straps or wires will be utilized for cell interconnects rather than the flexible circuit sheet now in use. With solar cells having patterned back metal, interconnect contacts to the fronts and backs of cells will be very similar.

3.1.10 STEP ELEVEN: ENCAPSULATION

Encapsulation is necessary to support and protect the interconnected solar cells. Accordingly, it will play a very important role in module reliability as well as in the performance of the interconnected cells.

Major failure modes for modules are expected to be related to the solar cell interconnections. It is probable that, until there is sufficient evidence that an interconnected group of cells can meet a greater than 20 year MTBF reliability criterion without any encapsulation, the cells must be encapsulated in such a way as to offer a considerable degree of protection from the environment if 20 year MTBF is to be achieved. (Indeed, the degree of reliability required for low cost per watt-hour modules is so high that it will probably be best accomplished by incorporation of high reliability concepts in both metallization/interconnect and encapsulation.) Such overall protection requires both front and back protection for the cells with a material impervious to moisture and other contaminants, and, most important, a high quality edge gasket having excellent sealing properties. The front protection must be transparent and have proven terrestrial environment reliability. The back plate may or may not be transparent, must have good thermal conduction, and also have proven terrestrial reliability.

Together, the two must provide structural support for module handling and environmental mechanical stress such as wind loading. Glass meets all requirements for both front and back, except for good thermal conductivity for the back. A glass front cover and a steel back plate is the basis of the encapsulation scheme utilized in this study.

Within the protecting glass cover and steel back plate, the solar cells must be effectively coupled optically through the front surface and efficiently connected thermally to the back plate. (Thermal connection to the front surface is also necessary in order to minimize cell operating temperatures.) The volume surrounding the interconnected cells is, thus, filled with a silicone gel which is optically clear, coupling the cells to the front surface both optically and thermally, while providing a good thermal path from the cell interconnection to the steel back. The silicone also acts as a secondary barrier to moisture and contamination ingression.

Additional structural strength, as well as a seat for location of the primary ingression barrier, is provided by a steel bezel which overlaps both the steel back plate and the glass cover. The regions of overlap provide the primary seal for the module, utilizing a formed-in-place gasket.

The encapsulation, thus, is provided by a glass cover, a steel back and bezel, a silicone gel surrounding the interconnected cells, and a formed-in-place gasket at the module perimeter. Physically, the encapsulation step starts with assembly of the glass cover, interconnected cells, and steel back. This assembly is then back-filled, under vacuum, with silicone gel, and the gel is cured to a pliable consistency. The bezel is then attached with the formed-in-place gasketing being applied around the periphery of the glass cover and steel back plate. The gasket, held in place by the bezel, is then cured to its final condition.

This process is more expensive (in that it utilizes more materials) than a single sided encapsulation system. However, with today's limited reliability

experience, this added expense is probably necessary to ensure a 20 year life for solar cell modules. Further, this proposed process step is conservative in that, if it is proven to be excessively wasteful of materials in the future, a less sophisticated encapsulant scheme is easily substituted. Present implementation of a simpler encapsulation technique will neither help ensure future reliability nor establish the necessary manufacturing experience for future reliable encapsulation technology. It should be emphasized that such a sophisticated encapsulation system is still capable of meeting the 1985 LSSA Project price goal of 50¢/watt for complete modules. Projected prices for encapsulation materials total less than $\$2/ft^2$, and, with automated assembly of 15% solar modules, the encapsulation costs will still be only about 1/3 of the total.

3.1.11 PROCESS SEQUENCE RATIONALE AND INTERRELATIONS BETWEEN PROCESS STEPS

The individual process steps of the process sequence have been presented in Sections 3.1.1 - 3.1.10. Each individual step is interactive in a manner with the other steps to provide an optimally efficient, cost effective solar cell and module. The process sequence has been chosen from processes with proven technical feasibility, which have, at the same time, the potential of meeting the long range cost goals.

Processes have been chosen such that consumed materials are minimized and, in addition, are additive in nature, that is, utilized to build upon the cell structure (and performance) rather than being partially removed and discarded as waste materials. Where feasible, consumed materials are recycled within the process. Waste disposal is also minimized through the use of dry plasma processing where practicable.

The process sequence is initiated with a dry plasma etching of the starting material surfaces. This ensures a smooth surface for the back of the cell, and also that any poor quality silicon at the surface of a wafer or ribbon, caused either by contamination or damage, is removed. The smooth back surface, in conjunction with a textured front surface allows total internal reflection of light. This reflection, in turn, reduces the silicon thickness necessary to assure efficient light absorption within the cell necessary for high solar cell conversion efficiency. Light reflecting back to the front surface will, for the most part, be transmitted out of the cell. Longer infrared wavelengths, to which silicon is transparent, will thus pass out of the cell without being absorbed, reducing the cell operating temperature compared with absorbing back surfaces of currently produced solar cell structures.

In order to maintain the smooth back surface during texture etching of the front surface, a wax resist is applied. Following texture etching this wax resist is reclaimed. Reclaiming of the wax will be less than 100% efficient, of course, but the costs of consumed materials are minimized and waste disposal virtually eliminated by this process sequence.

Texture etching is a wet chemistry step. This etching is performed in an alkaline solution, with most of the chemicals consumed before bath replacement. The benefits gained from texture etched surfaces make this wet chemistry step extremely cost effective.

The textured surface, in addition to expediting the back surface reflection effects already discussed, has other profound effects on cell operation and on processing. Very shallow p-n junctions are achievable by ion implantation. The general light-trapping nature of a textured surface increases efficiency appreciably. The textured surface also allows utilization of an antireflection coating with a somewhat lower index of refraction than would be optimum for a

smooth front surface. This feature permits the use of silicon nitride with an index of refraction near 2.0 as the antireflection coating.

Silicon nitride serves many functions in addition to its effective use as an antireflection coating. It acts as a surface and p-n junction passivant. The silicon nitride also serves as a plating mask, for both front and back surfaces, allowing minimum metal consumption for metallizing both surfaces while enhancing back surface reflection.

The combination of a textured front surface, and a smooth back surface with reflection occurring from its unmetallized areas, allows the utilization of thinner silicon material than could otherwise be achieved. If, for example, efficient reflection of light can be achieved from the back surface, and accounting for the increased path length of light in the silicon from refraction at the front textured surface, less than one-half of the silicon thickness is required to absorb the same amount of light as is needed for a solar cell with a smooth front surface and having no back reflection. This factor will obviously reduce the cost of input silicon by permitting use of thinner substrates to make high efficiency cells.

Patterning of the silicon nitride dielectric layer is accomplished without the use of photoresist chemicals and solvents. Further, no photoresist removal step is required, further eliminating material consumption while gaining process simplicity. The dry plasma etching technique utilizing mechanical masking also provides edge protection, if desired, allowing total areal usage of the silicon sheet while maintaining a passivated p-n junction. Masked plasma etching allows simultaneous front and back patterning of the silicon sheet, further simplifying the process sequence while optimizing solar cell efficiency and minimizing consumed materials.

Ion implantation, in addition to providing p-n junction advantages already discussed, ensures that only the desired dopant species are put into the silicon, eliminating possible incorporation of undesirable impurities into the area of the illuminated p-n junction. This aspect, as well as other inherent control features

of ion implantation, should result in a process with as excellent a distribution of solar cell outputs as the quality of the input material is capable of providing.

The only high temperature steps in the process sequence are silicon nitride deposition and anneal. It appears possible to combine these steps; in any case, both the front surface p-n junction and the back surface high-low junction are activated simultaneously.

Metallization by plating is an additive process in that metal is deposited only where it is ultimately utilized. The combination of palladium silicide-nickel-solder also has the potential of being an extremely reliable metallization system, allowing the 20 year reliability goal to be met or surpassed. While this is presently unproven, this metallization system may allow reduced encapsulation requirements and, thus, reduced encapsulation costs.

The interconnection scheme is versatile with respect to solar cell size and shape as well as method of cell interconnection (series, series-parallel, or parallel). Further, it has multiple contact and low electrical loss capability, while also being of low labor content now and capable of full automation in the future.

The module encapsulation approach is conservative for the sake of reliability. Future developments may ease the requirements for encapsulation, simplifying this technique at that time. Most important, being the last step, it is the least interactive with other steps in the process sequence, and will move only in the direction of simplification, not increased complexity.

Each step of the process sequence, thus, contributes to the cell and module in several ways. Consumed materials are intentionally kept low, substituting advanced technologies for traditonally more expensive (though technically

feasible) steps. Further, the process is capable of utilizing as-grown silicon sheet material with no penalty compared to sliced Cz material.

3.2 WAX RESIST TECHNOLOGY ADVANCEMENT

Two separate wax masking technologies have been developed during this contract. First, a wax-solvent system was developed which was capable of satisfying the goals of the contract. After a limited use of this technology, a more cost effective process which utilizes melted wax was developed. These technologies are presented in this section.

3.2.1 WAX-SOLVENT TECHNOLOGY

The study of a wax and solvent system for masking against texture etching solutions (as well as other chemical solutions) is presented in this section. Satisfactory results from the standpoints of processing, economy, and environmental impact have been achieved with a wax-solvent masking system.

3.2.1.1 SELECTION OF THE WAX

In order to effect a substantial cost reduction in wafer processing, an inexpensive and effective alternative to the presently used photoresist was sought. A preliminary survey of available materials revealed that several of the many commercial waxes met the most basic requirements of availability, economy, and lack of toxicity.

The substance to be used has additional criteria to meet:

a. chemical inertness

b. physical durability

c. ease of application

d. recoverability

The most demanding conditions to be met are those imposed by the chemical behavior requirements. The use of halogenating and oxidizing acid etches

eliminates many candidate materials from further consideration. A most severe set of conditions is posed by the intended use of wax in a texture etch process. The preferred etch formulations, from the viewpoints of safety and economy, are those based on hot alkali hydroxide solutions. The common animal and vegetable waxes are chemically classified as esters. Esters are susceptable to a spontaneous and, for practical purposes, irreversible degradation reaction with hot alkali hydroxides in which the ester is converted to an alcohol and the soluble alkali salt of a fatty acid. So readily does the reaction occur that a similar process is used to manufacture soap - the sodium salt of various fatty acids derived from tallow or vegetable matter.

This consideration narrowed the range of acceptable waxes to those derived from petroleum, of which there are two types: paraffin and microcrystalline waxes. These waxes are composed of saturated hydrocarbons rather than esters and are thus immune to the degradation described above. These waxes are also resistant to the halogenating and oxidizing reagents used in solar cell manufacture. While either type appears satisfactory, additional requirements must be considered. The wax used should have good mechanical strength in the form of hardness and a high melting or softening point to resist removal by heated processing reagents. The paraffin waxes have, as a class, low melting points. They also tend to soften appreciably below their melting points, and are rather soft even at room temperature. The microcrystalline waxes, however, display properties that are excellently suited for wafer masking. They are very hard at low temperatures and retain their hardness until the melting point is reached. The melting point is sharp, with no premature softening. The chemical inertness, as discussed, is exceptional, resisting attack by every non-solvent reagent used in the current (or anticipated) processing sequence. A very high melting point can be specified for micro-

crystalline wax to withstand those reagents used at elevated temperatures. Microcrystalline waxes possess yet other desirable properties. Being obtained from mineral sources, they are not susceptable to attack by micro-organisms which would decay waxes derived from organic sources.

The wax chosen -- Multiwax 195-M microcrystalline wax -- was investigated for application to silicon wafers. This wax, which melts at 90°C, may be dissolved in a limited variety of organic solvents so that application can be achieved at room temperature through the use of low-viscosity solutions. Multiwax 195-M has been found to adhere tenaciously to bare silicon, silicon dioxide, and silicon nitride. The use of a soluble wax also allows convenient removal from cells after processing.

The extremely high boiling range for the chosen wax permits easy and effective recovery from solvents used to remove wax after processing by the use of a simple one-step distillation. Precipitation of wax from chilled solvent is also possible, and allows indefinite recycling of wax which appreciably reduces costs and conserves material.

3.2.1.2 SOLVENT-WAX SOLUTIONS

One method of applying and removing masking wax from wafers is by means of an organic solvent. A solution of wax in solvent provides an easily dispensed and stored liquid masking agent which, when applied, will form a solid wax coating as the volatile solvent evaporates. Unlike the application of pure wax, no melting is required and immediate use at room temperature is possible. Additionally, the selection of a suitable solvent allows adjustment of density and viscosity of the solution over a wide range to permit optimum processing properties with a variety of application methods. An interesting feature of the solvent technique is the possibility of large-scale recycling of materials, eliminating the need for purification of spent solvent, and significantly reducing waste stream volume.

3.2.1.2.1 SOLUBILITY

The microcrystalline wax used, Multiwax 195-M, is soluble in a number of easily available solvents. The data on solubility are summarized in Table 1 and Figure 1. The solubility values are for saturated solutions of wax in various solvents now in use by the semiconductor industry for other processes, avoiding exotic and costly special materials.

The choice of solvent depends on such factors as solvent cost and availability, and the particular demands of the application method in terms of the masking solution physical properties. It has been found that the most successful wax films are produced by the use of the most concentrated solutions, i.e. those using trichloroethylene. It must be noted however, that the use of some of the less effective solvents is acceptable. The first four solvents listed in Table 1 provide satisfactory results. The wide variety of possible solvents ensures that restriction in the use of certain solvents for health or environmental reasons will have little impact on implementation of the method, since substitute solvents are available.

The preparation of a masking solution is simple--an excess of wax is added to the desired solvent and allowed to dissolve with agitation at room temperature. Large volumes of solution can be conveniently prepared in a matter of hours with very modest equipment.

It is seen from these data that a several-fold increase in solubility is effected by elevated solvent temperatures. These solubility differences lend themselves to certain processing operations and are discussed below.

3.2.1.2.2 APPLICATION AND REMOVAL

Application of Multiwax 195-M has been achieved by the use of room temperature saturated solvent-wax solutions. The two most successful techniques are spin-on

TABLE 1

SOLUBILITY OF MULTIWAX 195-M IN SELECTED SOLVENTS

SOLVENT	GRAMS PER MILLILITER OF WAX - SOLVENT SOLUTION	
	23°C	80°C
trichloroethylene	0.052	0.246
methyl ethyl ketone	0.032	--
toluene	0.026	0.1624
1,1,1-trichloroethane	0.023	--
1,3,5-trimethylbenzene	0.020	0.106
xylene	0.017	0.149
naphtha	0.0172	0.098
perchloroethylene	0.011	--
methylene chloride	0.0079	--
butyl acetate	0.0069	0.0457

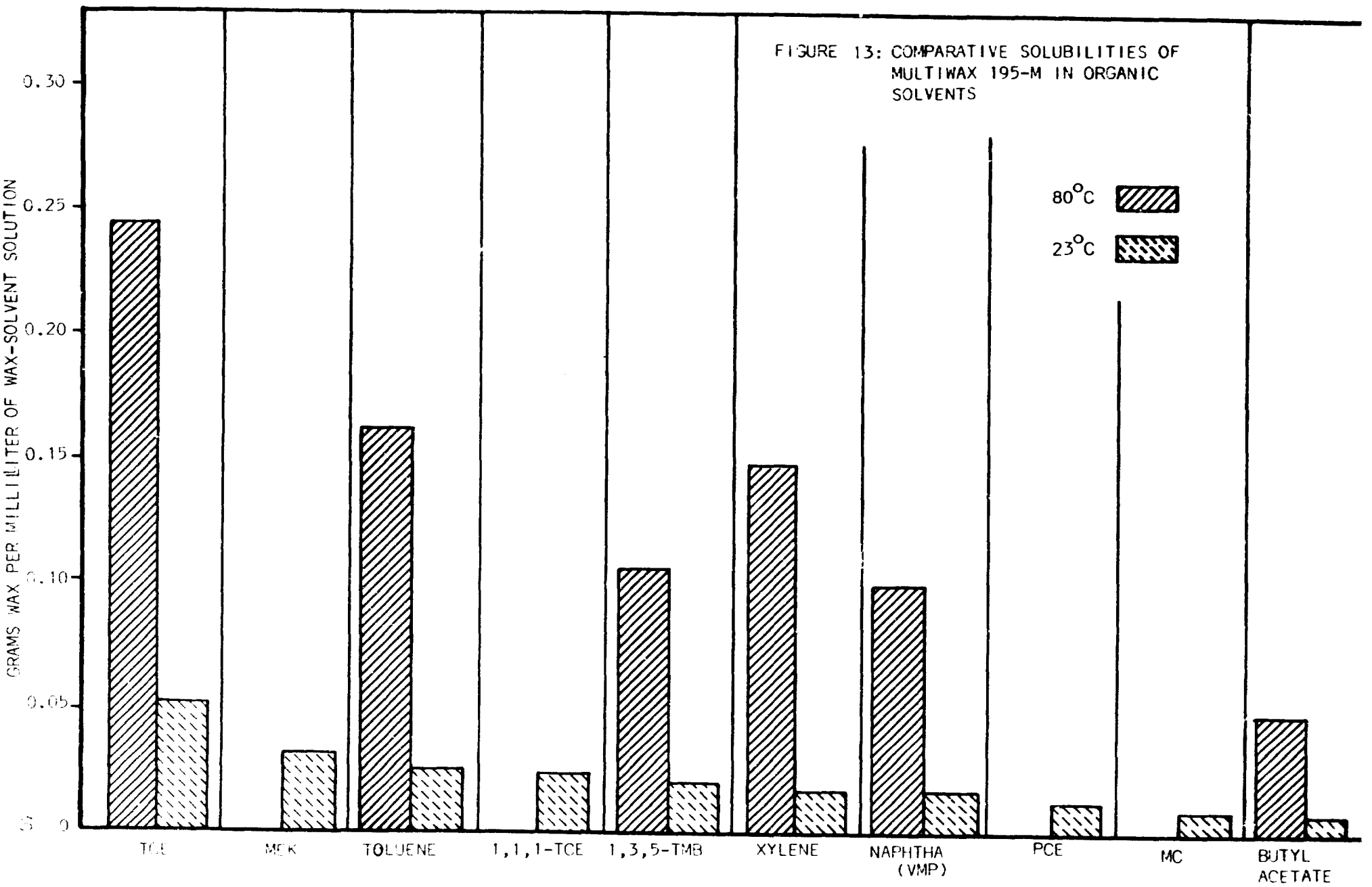


FIGURE 13: COMPARATIVE SOLUBILITIES OF MULTIWAX 195-M IN ORGANIC SOLVENTS

and paint-on. In the spinning method, the solution is applied to a cell which is spun rapidly, producing a thin even film. The paint-on method involves manual application of solution by means of a brush. The latter method is particularly useful for processing very large or oddly-shaped cells such as those fabricated from ribbons. It is expected that a large wick application and automated transport system can be adapted to the high volume processing of ribbons to eliminate manual applications.

After the solution is applied, a dry-off step has been found necessary to allow evaporation of the solvent. This has been performed by hot air blast, cold air blast, baking, and infrared heating, with roughly equivalent results. If the evaporation step is carried out in an enclosed fixture, removal of solvent vapors is possible. This can be accomplished by several methods -- e.g. absorption by activated carbon, removal by cold condensation, or dissolution by an oil mask in the exhaust stream. The recovered solvent can then be re-used.

The sequence for wax removal after processing offers several alternative approaches. Dissolution of wax by cold, fresh solvent is possible. It has been found, however, that more efficient and complete removal is effected by means of heated solvents. This approach has been successfully tested and found to be practical. A soak in two or three hot solvent baths will remove all but traces of wax, which are, in turn, eliminated by a standard oxygen plasma cleaning step. The use of solvents for removal of wax also offers recycle possibilities. Wax-laden solvent, when allowed to cool, precipitates excess wax, forming a saturated wax solution at room temperature that can be used without modification as the masking solution for incoming cell substrates.

The separation of precipitated wax is readily accomplished by means of filters or, more advantageously, by the use of continuous centrifuges similar to those used in the dairy industry for the separation of cream from milk. Precipitated wax is combined with recovered solvent from the evaporation system to produce additional masking solution.

3.2.2 MELTED WAX MASKING

The utilization of solvents to dissolve the wax for application to the substrates has some drawbacks. The most efficient solvents have undesirable environmental impacts. The wax-solvent solutions require preparation, adding slightly of the cost of the process and ultimately of the solar cell. Further, the solvents are an expense themselves; while partiallly recoverable, some part of the solvent is consumed in the process.

Efforts were thus, made to investigate alternatives to applying wax from a wax-solvent solution. A melted wax application proved to be a satisfactory process.

The wax selected fo use in solvent-wax masking solutions, Multiwax 195M melts at 90°C, forming a low viscosity liquid which is easily handled. The availability of inexpensive equipment to attain and maintain the melting temperature of this wax suggested use of this wax for application in melted form.

3.2.2.1 ADVANTAGES AND DISADVANTAGES OF MELTED WAX APPLICATION

The first apparent advantage to the melted wax method is that of convenience. The wax, as delivered, is a hard solid. Preparation of the solvent-wax solutions involves the crushing of the wax and mixing with a suitable solvent. The duration

of the mixing process is relatively long--several hours-- and is required to achieve a saturated solution of wax in the solvent (necessary for process control). With a melted wax system, the masking agent is in usable form as received from the manufacturer, with the only preparation being that of melting. In addition to the convenience of ready use, the time-consuming solution preparation step is eliminated.

The cost savings effected by reduction of preparation time are further increased by elimination of the required solvents. All of the solvents found to be effective in forming wax solutions are derived from petroleum and are likely to suffer from both decreased supply and increased price in the future. Use of wax solutions also demands evaporation of solvent from the wax coating after application. Although recovery of vaporized solvent is possible, the process is neither cost-free nor totally effective. Recovery also involves reclamation of the solvent in reuseable form -- a complication to the process.

With any solvent-based process, the consequences of personnel exposure must be considered. All of the acceptable solvents are volatile, odiferous, and toxic. Some are flammable. Worker exposure to solvent fumes at some point in processing seems inevitable. Even though proper ventilation can reduce exposure, and reclamation can greatly reduce the amount of lost solvent, it is inevitable that some solvent will be discharged to the atmosphere -- an ecologically undesirable situation.

Aside from eliminating the cost and environmental problems of solvent use, melted wax offers improvement of masking performance. Direct application of melted wax results in a thicker, denser wax coating than can be readily achieved through the use of wax solutions. Although coatings produced by solvent solutions have been found satisfactory in limited laboratory production,

the large-scale use of the process implies the need for more stringent process controls, especially for textured surfaces. The thick, dense coating produced by direct application of liquid wax ensures improved masking performance.

Application of a melted wax eliminates the requirement of drying the layer applied from a wax-solvent system. This elimination of solvent removal from the mask layer also affords added reliability, through a decrease in masking defects seen in any solid-solvent system (including photoresist materials). In efforts to decrease the time necessary for the solvent drive-out required by the use of solvent-wax solutions, higher temperatures and vacuum drying techniques were researched. It has been found that certain conditions of temperature and vacuum, either alone or in combination, caused the eruption of solvent vapor bubbles within the wax layer, resulting in porosity and pinhole defects through the masking layer. Use of pure wax, from which no solvents are removed, eliminates this problem.

The use of liquid wax does present some problems. After application to a surface, the wax tends to shrink upon cooling, tending to withdraw slightly from the edges of the coated surface. The application of a thicker wax coating also implies increased difficulty in removing the coating after processing. These disadvantages have already been largely overcome, as will be discussed later.

5.2.2.2 APPLICATION OF MELTED WAX

The melted wax may be applied by any of the methods useful for solvent-wax solutions. All wafer surfaces encountered in cell manufacture are easily wet by wax, e.g., bare silicon, silicon dioxide, silicon nitride, and various deposited and applied masking and dopant glasses.

Direct printing of melted wax on cell surfaces has proven successful, as has spray application. In both cases, heating of the entire substrate has been found advantageous.

A straightforward method of application to round substrates is by spinning. A standard photoresist spinner is used in this method. The cell is placed on a vacuum chuck and a small quantity of liquid wax is applied. Rapid rotation of the cell then produces a smooth, level wax coating. The availability of automatic photoresist equipment makes this technique immediately applicable with present equipment, although to produce optimum results, minor modifications are desirable. Automatic dispensers for photoresist need only be heated, for example, by wrapping with heating tape to allow delivery of melted wax. Heating of the cell surface has been found to produce more consistant results than the use of unheated surfaces. This has been done with hot air, but may be accomplished in numerous ways. Cooling of the cell to harden the applied coating may be necessary and can be conveniently arranged by use of a cool air stream directed at the cells as they leave the spinner chuck. One additional modification completes the system. As the cell is spun to level the wax, excess wax is thrown from the wafer, collecting and solidifing in the spinner shield. Heating of this shield allows the wax to flow back into the wax supply receptacle for reuse.

For irregularly shaped cells which cannot be spun, such as ribbon substrates, alternate application techniques have been investigated. In its simplest form, application is effected by covering a glass or ceramic plate with a film of melted wax and manually pressing the cell surface against the plate. This method produces a continuous film without wetting the back of the cell. Although the wax layer produced in this way is somewhat more uneven than that obtained by spinning, the uneveness does not hinder masking performance. Refinement of the method should allow automation of the process. Use of a

rotating porcelain cylinder dipping into a pool of melted wax has proven practical. The rotating cylinder, easily wet by wax, acquires a thin, continuous film which is transferred to the cell surface upon contact.

As mentioned previously, a problem encountered with the use of melted wax is that of shrinkage. This has been alleviated by the use of appropriate fillers in the wax. The fillers used are finely powdered substances that produce a suspension of solid particles in the wax, promoting dimensional stability. The successful filler material should be insoluble in water and the commonly used acid etchants, be soft enough to avoid abrading the cell surface, and be readily available at low cost. The common mineral, fluorite (calcium fluoride) fulfills each of these requirements, and has been used with success in our experiments.

3.2.2.3 REMOVAL OF WAX

Removal of the wax coating can be accomplished, as with the wax-solvent system, by dissolution with solvents. The use of thicker wax coatings produced by melted wax, and the incorporation of filler materials into the wax, does present problems, however. For example, the use of greater amounts of solvent than is customary with the thin solvent-wax solution films will be required to effectively remove melted wax films. Any filler material in the wax will simply settle to the bottom of the solvent container. The solvent and wax can be separated from each other by distillation, during which the filler will remain with the wax, making reformulation unnecessary. The use of solvents, nevertheless, is undesirable for the reasons given earlier.

An alternate removal process which avoids solvent use entirely has been investigated. It has been found that wax can be removed from cell surfaces by immersion of the cells in hot water, during which the wax melts and floats to

the surface in an easily removed layer. The process is incomplete when pure water at its boiling point is used; about 70% of the applied wax is removed. Addition of dense salts such as ammonium sulfate to the water raises the boiling temperature and density of the water so that more complete removal results.

This technique is also capable of automation. Currently available equipment exists that cleans silicon wafers by directing a high pressure stream of water onto the wafer surface. Simple modification will result in a device that produces a stream of hot water that will effectively remove the wax from the cell surface. The water-wax mixture that results can be directed into a settling tank where the immiscibility of the wax and water (and their density differences) will cause separation of the wax into a floating layer upon the water. If the tank is heated, the wax can be drawn off as a liquid for use in masking incoming cells. The water solution can also be reused, resulting in essentially no waste of any materials. In preliminary tests of this technique, separation of filler material from the wax has been shown to be small.

The traces of wax that remain on a cell surface after the water clean process can be removed by an oxygen plasma, which would normally be utilized prior to either ion implantation or silicon nitride deposition, the next steps in the process sequence.

3.3 PLASMA ETCHING OF SILICON AND SILICON NITRIDE

Processing of solar cells can involve a large number and variety of wet chemistry steps. These steps include such items as isotropic silicon etching to remove saw damage or surface layers of poor quality, texture (anisotropic) etching of silicon, dielectric etching, metal etching, and metal plating. Wet chemical steps may be the only viable means of achieving the desired result in some cases, such as texture etching and metal plating. In other cases,

however, alternatives have been identified which may achieve the desired result while minimizing consumed materials and waste disp , requirements. Two such alternatives are the plasma etching of silicon to remove sawing damage (or other undesirable surface layers), and the plasma etching of patterns in silicon nitride without utilizing photoresist.

Plasma processing utilizes an appropriate gas (or gas mixture) at a reduced pressure, ionized in an RF field. The ions exist at low physical temperatures, but are highly energetic, representative of much higher effective temperatures. Surface processes which would normally require high temperatures can, thus, be performed at or near room temperature.

3.3.1 ETCHANT GASES AND REACTION MECHANISM

The application of plasma technology has become widespread in the semiconductor industry (1). Until recently, however, little was known about the actual chemical mechanism of silicon and silicon dioxide etching in a glow discharge of a CF_4 / oxygen gas mixture. It was thought that the active species of fluorine chemically reacted with silicon to form volatile SiF_4 which was removed by the vacuum pump. Empirically it was found that the addition of oxygen accelerated this reaction. Spectroscopy of the reaction effluent gas and in situ Auger surface analysis (2,3) has provided considerable information about the reaction mechanism. This information has been used to develop a simple reaction model which can be substantiated by various reported experimental observations (4).

In the absence of oxygen, the overall reaction for etching silicon can be written as:

$$4\ CF_4 + Si \rightarrow 2C_2F_6 + SiF_4.$$

The reaction rate is determined by the difference between the generation rate of active species and their recombination rate. Reactive species, mainly CF_3 and F, are formed by electron-impact-dissociation in the gas phase and are absorbed on the silicon surface where they either chemically react with silicon or recombine to form CF_4 or C_2F_6 by the reactions:

$$CF_3 + F \rightarrow CF_4$$

and

$$2\ CF_3 \rightarrow C_2F_6\ .$$

The concentration of the C_2F_6 species has been found to be the major controlling etch-rate factor, establishing reactant fluorine ions through the overall reaction:

$$2\ CF_4 \rightarrow C_2F_6 + 2F.$$

Other reactions, generating many other possible combinations of carbon and fluorine also occur. Formation of elemental carbon, which can deposit upon the silicon surface, will slow the etching reactions.

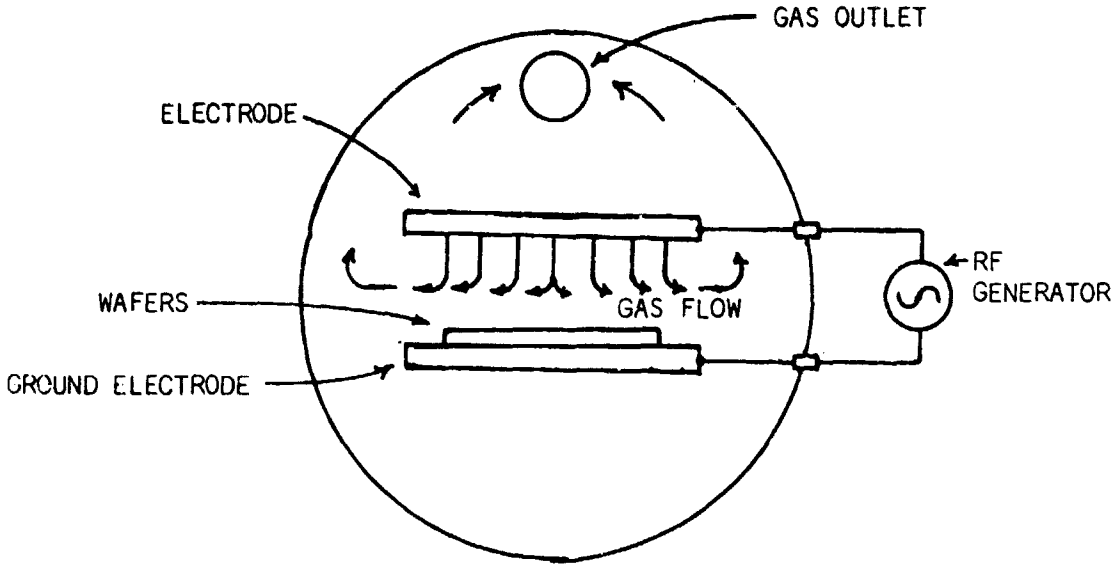
The addition of oxygen to the CF_4 plasma causes an increase in the etch rate by reducing the recombination rate of the active species. For given reaction conditions, the generation rate has been shown to be unaffected by the addition of oxygen. However, the oxygen reacts with the absorbed carbon (and carbon species) to form volatile CO, CO_2, and some COF_2. This greatly reduces the recombination of CF_3 into C_2F_6, allowing much more of the absorbed fluorine to react with silicon. This model can be demonstrated by "loading effect" experiments. These experiments show that the etch rate of silicon dioxide in CF_4 is relatively insensitive to wafer area, but silicon etch rates decrease rapidly with increased area. When etching silicon dioxide, the oxygen reaction product forms volatile CO and CO_2. Using these concepts, a quantitative etch rate model has been developed as a function of area, reactive species generation rate, and oxygen concentration (4). The generation rate is

determined by process parameters such as power, gas pressure, and temperature. This model was developed using Si and SiO_2 etching by CF_4/O_2, but should be easily applied to other systems once the reaction products are identified.

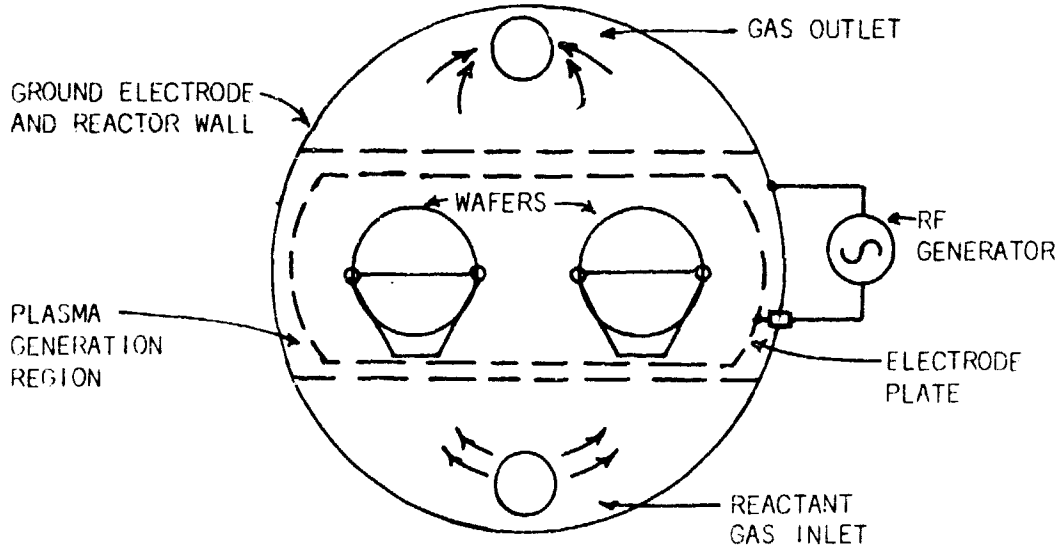
Another recent development is the correlation between optical intensity of atomic fluorine emission of the reactant plasma and the etching reaction (3,6). There is a direct correlation between the emission intensity and etch rate. Not only does this give an in-process measurement of etch rate which can be used to optimize the etch process, but it also gives a sharp indication of changes in the reaction rate. The latter observation has been incorporated into commercial plasma equipment to detect the etch completion of a thin film. This "end-point" detection has greatly improved the control of etching processes of thin films such as silicon nitride. Also, a similar effect is observed while etching mechanically damaged (as-sawn) silicon wafers and may possibly be used to monitor this process as well (6).

3.3.2 EQUIPMENT

Two types of plasma reactors are being used in this study -- a parallel plate reactor with the wafers directly in the RF field, and a capacitance-coupled reactor with the wafers outside of the RF field. Schematic diagrams of these reactor types are shown in Figure 2. In the parallel plate reactor, the reactant gas is dispensed through small openings in the top electrode and the wafer is placed on the bottom (ground potential) plate. An RF field applied across these plates generates a glow discharge above the wafer. The gas is exhausted around the edge of the plates. The capacitance-coupled plasma system is a "barrel" or "tunnel" reactor with the reactant gas introduced at the bottom of the chamber and exhausted at the top. The wafers are placed inside a "barrel" electrode and the RF field is applied between it and the aluminum reactor wall



(a) Parallel Plate Reactor



(b) Capacitance-Coupled RF,
or Tunnel, Reactor

FIGURE 2: SCHEMATIC CONFIGURATIONS OF PLASMA REACTOR TYPES: (a) PARALLEL PLATE REACTOR, (b) CAPACITANCE COUPLED RF (OR TUNNEL) REACTOR.

which is at ground potential. The cross gas flow enhances the diffusion of the reactant species from the field region to the wafers. Both reactors have a 300 watt RF generator, automatic process timer, and optical end-point detection.

3.3.3 SILICON ETCHING

Etching of silicon in a plasma has been studied with a mixture of CF_4 and O_2 in a parallel plate plasma chamber. The parallel plate reactor offers better uniformity and generally higher etch rates than other reactor configurations. In these reactors, the wafers are laid on the bottom electrode. As a result, these reactions etch only one side of the wafers since no etching occurs where a wafer is supported on its back. Currently, commercial equipment will process 25 wafers per run, half the number of a tunnel reactor, and costs 3 times as much. In order to make this a cost effective, viable process for silicon damage removal, the throughput must be appreciably increased.

As predicted by the plasma reaction model, high etch rates can be obtained at higher power rates, i.e. higher generation of active species. But to increase the etch rate, the recombination rate must be decreased by increasing the oxygen to CF_4 ratio. This has been verified at 800 watts of power which required about a 30% oxygen mixture compared to 8% normally used at lower power levels to maximize the etch rate (6). The major problem experienced with etching silicon in a parallel plate reactor has been the rapid decrease of etch rate with increased wafer loading (5). Use of higher power and oxygen ratio should improve the etch rate loading effect, and this is currently being evaluated. We have verified reported etch rates using CF_4/8% O_2 at 300 watts.

For the process sequence being developed during this contract, there is no requirement to etch both sides of silicon substrates, since one side of the cell will be texture etched before a high temperature operation. The

possibility of plasma etching only one side is therefore being considered for the proposed process. This may make current plasma equipment and processing cost effective for solar cell application.

The one side silicon etch process in a tunnel reactor offers another alternative to the parallel plate reactor. When the wafers are loaded back to back, the exposed side only will be etched in a tunnel reactor. Increased spacing can be used to improve etch uniformity which may not be as critical for solar cell application as it is for other silicon devices and integrated circuits. Also, reducing the surface area by half should increase the etch rate. If spacing is maintained the same, combined with increased capacity (50 wafers versus 25 per run), reduced labor, and reduced equipment cost, a sufficient etch rate could result in a much lower cost process. This configuration must be further evaluated to determine achievable etch rates.

The amount of plasma removal of mechanically damaged layers on as-sawn silicon wafers affects not only solar cell performance but equipment throughput. In general industry procedures, as much as 1½ mils (37 microns) is currently being removed from each side of a sawed silicon wafer. This amount of material removal may not be required for solar cell fabrication, but a precise amount depends upon the sawing technology utilized. Plasma removal of the back-side saw damage has been demonstrated to be all that is necessary if the front side is texture etched, since excellent solar cells have been processed using the wet chemistry texture etch to remove saw damage layers on both surfaces before high-temperature processing.

3.3.4 SILICON NITRIDE ETCHING

Efforts to develop a mechanical etch mask of the silicon nitride film for plated solar cell metallization has concentrated on obtaining adequate

geometric resolution. Resolution includes the mask-to-etch line dimension ratio, and the sharpness of the etch step. Mask-to-etch line dimension ratio and its controllability determine the geometric tolerance needed for the mask. This tolerance can impact the effort required to produce the metal mask. For example, if the line etches much wider than the mask opening, a smaller mask opening will become more difficult to make and will require thinner masks. Also, the sharpness of the etch step will affect the final quality of the process. A sharp etch step is desirable to maximize contact area and metal adherence for a given metallized line width.

Thin metal masks, conventionally used to define a metal evaporation pattern, have been evaluated to demonstrate attainable etching resolution. These masks were 0.015 inch thick stainless steel and molybdenum. Cold-rolled steel masks as thin as 0.006 inch have also been utilized. Aluminum can also be used and is desirable for its resistance to CF_4 plasma attack.

Uniform contact or spacing between the mask and the silicon substrate becomes increasingly difficult as the mask becomes thinner. Very thin masks, in fact bend easily. Two methods have been studied: 1) utilizing a magnetic mask and hold-down and 2) utilizing a silk-screen type mask.

For patterning only one side of the wafer, the magnetic mask and hold-down have worked very well. Double sided patterning appears readily performed by backing one or both masks with magnets, the magnets being spaced between the pattern openings. Closed geometry metallization patterns must, however, be modified to permit bridging so that the mask can remain contiguous.

Screen printing masks that use a thin metallic pattern mounted on stainless steel screen are commonly used to apply metal paste, inks, resists, etc. in electronic devices (7). The screen provides mechanical support while the thin, etched metal mask defines the pattern. The metal is mounted to the screen and

then etched; this provides the flexibility of closed geometries. This could eliminate any requirement for redesign of closed geometry metallization patterns. Also, the deformation allowance in the screen should reduce potential wafer damage while providing better contact between the mask and the textured surface. mechanical mask is currently under evaluation; so are thicker metal masks.

Two methods of patterning silicon nitride by plasma etching with a mechanical mask have been investigated. One results in a positive replication of the mask (in the silicon nitride), and the other results in a negative replication of the mask.

3.3.4.1 ETCHING THROUGH OPENINGS IN THE MASK (POSITIVE PROCESS)

The process of etching through openings in a mechanical mask is completely analogous to the process widely utilized in the semiconductor industry of etching through openings in a photoresist pattern. In the positive plasma process, openings are made in the mechanical mask where nitride will be removed from the substrate. The mechanical mask is held in close proximity to the substrate and placed within the plasma chamber. The plasma gases, then, have unobstructed access to the areas of silicon nitride to be etched.

Pattern definition depends upon several factors. First, proximity of the mask to the wafers is important; if too large a gap exists, the pattern is broadened. Second, the pressure of gases within the plasma chamber is critical. Lower pressure (higher vacuum) leads directly to sharper pattern definition. Third, the energy level of the plasma is a key parameter in determining pattern definition; specifically, higher RF power results in better pattern definition.

Patterns have been successfully formed in Si_3N_4 through openings in a metal mask using CF_4 as the etchant gas on both smooth and textured surfaces. Excellent pattern definition has been achieved, but the repeatability of the process has varied. This indicates that the required level of control of the

important variables is still not complete. However, the excellent results obtained indicate that production readiness of the process is achievable with additional engineering efort.

3.3.4.2 ETCHING BENEATH THE METAL MASK (NEGATIVE PROCESS)

During the investigations of etching through openings in a metal mask, the metal mask was placed in contact with one of the RF electrodes. An unexpected result occurred: etching of the Si_3N_4 was restricted to areas actually beneath the metal pattern of the mask, leaving the areas exposed by the openings in the mask unetched.

By placing the metal mask in electrical contact with the RF plasma electrode, the mask itself becomes part of the electrode. Ionization of the gas is then concentrated between the mask and the wafer, maximizing etching there. This results in different optimization requirements for etching parameters (and key variables) than for the positive plasma etching method.

For negative plasma etching, it has been observed that etching can be non-uniform. Etching may occur most heavily at edges of the metal mask pattern, with less etching taking place beneath the metal mask. This effect becomes more pronounced as the width of the metal is increased. This presumably is due to a combination of field effects at the mask edge and gas availability as a function of distance beneath the mask. The width of the mask area to be replicated in the Si_3N_4 is the most critical parameter observed to date.

Results of negative plasma etching technique must still be classified as preliminary. Further developmental efforts are necessary to fully define the process.

3.3.4.3 RESULTS

Plasma patterning of a silicon nitride layer deposited on a textured silicon surface has now been achieved through openings in a mechanical mask with excellent pattern reproduction. Pattern dimensions in the silicon nitride layer are identical to corresponding dimensions in the mask, within measurement error. Patterning is accomplished with a one minute etch time. This is a major improvement over previous results in which pattern dimensions in the silicon nitride layer were 10% to 20% greater than mask dimensions.

The exact reproduction of pattern dimensions was obtained in a plasma reactor of the parallel plate configuration. For these experiments, a steel mask was placed over the silicon wafer and held against it by a magnet on the opposite side of the wafer.

The most important control parameter has been found to be the pressure within the plasma chamber; lower pressure allows better pattern reproduction. Present results have been obtained by the substitution of an improved vacuum pump for the pump originally on the system. This new vacuum pump, still a mechanical type, allows operating pressures as low as 0.05 torr, much lower than the original pump.

Two other operating parameters, mask proximity and power level, are important for process control, but appear much less critical than operating pressure. Mask proximity, in the present case, is obtained by a magnetic hold-down. The mask is in contact with the peaks of the textured surface, but not the valleys between the peaks. The nitride in the valleys still accurately replicated the mask, indicating that direct contact to the nitride is not mandatory. Independent varition of the power level has indicated that better control and replication occur at high power levels. These two factors, operating pressure and power, will be of great importance in future equipment designs.

The results to date are extremely encouraging. The process has now been developed well beyond the feasibility stage. Precise definition of the control parameters, however, is yet to be achieved, indicating the need for additional engineering efforts. The present knowledge and process performance indicate that production readiness of plasma patterning is achievable with additional engineering effort.

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5.4 REDUCED PRESSURE CHEMICAL VAPOR DEPOSITION OF SILICON NITRIDE

The deposition of thin layers of various materials is among the most important processes in the fabrication of semiconductor devices. These thin films are used for a variety of purposes including insulators, dielectric layers, diffusion and oxidation masking, and conductors. Through many refinements, the well-known chemical vapor deposition (CVD) method was applied to the semiconductor industry to produce these essential films. Developed in the 60's, deposition was performed in RF-powered reactors using horizontal susceptors for wafer heating and support. These "cold walled" systems were the main source of high quality films for silicon nitride and polycrystalline silicon. The very high capital and operating cost of these systems, however, soon prompted development of "Hot Wall" horizontal wafer deposition systems. Cheaper and more versatile, these systems were still limited in wafer throughput capacity. The latest development - CVD in a low pressure (vacuum CVD) system -- has removed the throughput limitation and improved uniformity.

This section presents a brief historical resume of this development and its application to the fabrication of silicon semiconductor devices with particular emphasis on solar cells. By applying data and observations obtained during the development of the first full scale production system for the deposition of silicon nitride, a quantitative analysis of the process was performed. Also, a theoretical discussion of the most important operating characteristics of vacuum CVD for depositing silicon nitride is presented.

The deposition system consists of a conventional diffusion furnace tube with vertically supported substrates. The kinetics of the low pressure, high velocity flow in the vacuum system provides greatly increased quality of the films, while vertical positioning of the substrates and conventional furnace equipment provide increased mass productivity and reduced cost.

Of major importance is the use of amorphous silicon nitride as an anti-reflection and junction protection coating for terrestrial silicon solar cells. Since its index of refraction is between that of glass and silicon, significant reduction in reflection loses can be achieved by a quarter wavelength thick layer of silicon nitride. When combined with its excellent barrier properties, the antireflective coating of CVD silicon nitride has assumed a paramount role in achieving cost effective solar energy goals. The vacuum CVD process provides the low cost and excellent thickness uniformity for this thin film application.

Generalized operating characteristics are discussed for the deposition of amorphous silicon nitride films from the following reaction of dichlorosilane an ammonia:

$$3\ SiH_2Cl_2 + 4\ NH_3 \rightarrow Si_3N_4 + 7\ HCl + 6\ H_2$$

A literature review revealed a lack of theoretical discussion concerning the changes in reaction kinetics compared to previous atmospheric pressure methods. Gas kinetic measurements were related to the special flow characteristics of the system. From deposition data, an activation energy for the above reaction was found to be 67.2 kcal/mole. A similar value was obtained assuming a second-order rate-determining reaction of the form:

$$SiH_2Cl_2 + NH_3 \rightarrow SiH_2(NH) + 2\ HCl$$

Also, normal chemical reaction theory does not accurately predict a mechanism, but discussion in this report indicates a gas-surface collision mechanism.

3.4.1 HISTORY OF CVD DEVELOPMENT

For many years, the cold wall RF reactor was virtually the only technique available for CVD of thin films used in silicon device processing. In the most common equipment geometry, the silicon wafers are placed on a flat graphite susceptor inside a rectangular cross-section quartz tube. Around the tube is a high power RF induction coil which heats the graphite susceptor to between

600° and 1000°C, as shown in Figure 3. The reactant gases mixed with a high volume of a carrier gas (H_2 or N_2) are injected into the front of the tube, and scavenger gases are exhausted out the rear of the tube, all near atmospheric pressure. As the cold gas mixture comes into contact with the hot wafers, a reaction takes place in a region about 1 cm above the wafer due to the laminar gas flow. The solid phase reactant deposits on the wafers. The flow kinetics of this system are very difficult to control; therefore, the most consistent deposition thickness displays 10 to 20% variation across a wafer and 30% average variation between wafers in the same deposition cycle. Also, the high volume of reactant and carrier gases combined with very large power consumption (a 100 kw. RF generator is used for large susceptors) and low wafer throughput makes this CVD method a very expensive and inefficient process.

In the early 1970's there was introduced a new system that provided a possible alternative to the RF systems. A "hot wall" CVD system was developed using a conventional diffusion furnace element to heat the wafers instead of the RF-induction heated susceptor. The cost savings in electrical power and equipment capital were very significant but the wafers were still in a horizontal position and this atmospheric process still required large volume gas flows. The aerodynamic factors of the tube and multi-tiered wafer carrier added more problems to controlling reaction kinetics; so the film uniformity and quality did not improve (1).

As an extension of the "hot wall" system, some early work was done on reduced pressure CVD of polycrystalline silicon thin films at Motorola (2). This system did obtain excellent quality films. Since then, work in this area proceeded towards utilization of lower pressures. The result was a system using a conventional diffusion tube (similar to the hot wall CVD system) by employing a very low gas flow into a vacuum system (3). The high velocity,

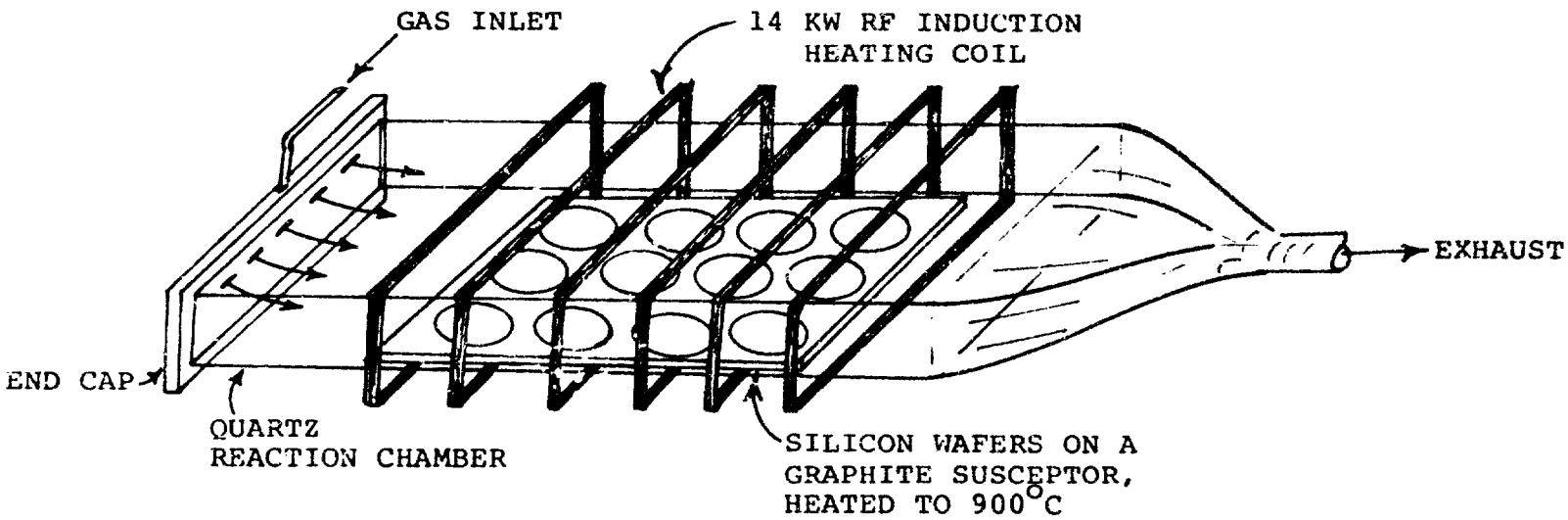


FIGURE 3: HORIZONTAL CVD REACTOR WITH RF INDUCTION HEATED WAFER SUSCEPTOR.

low pressure kinetics of this system provided a different deposition mechanism more closely dependent on random mean-free-path motion of reactant molecules instead of directional bulk flow patterns. This meant that the wafers could be oriented vertically, providing a many-fold increase in throughput, leading to the development of high volume production systems.

Development of these new systems was slow in coming. Research was begun at Motorola to evolve advanced vacuum CVD processes by expanding upon the earlier work on polysilicon films. The laboratory system revealed many technical problems such as short vacuum pump life, occasional hazy or poor film quality, and a lack of process control using silane and ammonia as reactants for silicon nitride. However, the steadily improving quality of the silicon nitride films produced in the laboratory eventually lead to the development of viable production systems.

3.1.2 PROCESS ADVANTAGES

Several mechanical and electrical properties of amorphous silicon nitride deposited using vacuum CVD show definite improvement and better controllability over previous deposition processes. Refractive index for thin, transparent films can be a direct indication of crystalline structure and impurity concentration. For amorphous silicon nitride, the refractive index should be 2.00 ± .02, and this is consistently achieved with vacuum CVD. However, on atmospheric pressure deposited films, the refractive index is in the range 1.95 ± .10 (4). The higher values (>2.05) approach that of bulk crystalline silicon nitride and can be interpreted as due to some short range crystallization in the film. The lower readings (<1.90) can be related to impurity levels, or a drastic change in the gas ratio which may affect the chemical structure. An example of an impurity is oxygen, forming an oxynitride compound which lowers the

refractive index towards that of pure silicon dioxide, 1.45. Either crystalline structure or oxynitride formation will lower the dielectric constant of the material. The dielectric constant of atmospheric pressure deposited silicon nitride is usually 6.5 (4), whereas vacuum CVD films have a higher constant of 7.3. The appearance of oxynitride in the film drastically increases the film's etching rate -- it is 2 to 3 times faster for a 20% oxynitride ratio. Variations in etch rates contribute to poor process and dimensional control of pattern generation. Besides very good thickness control, vacuum films of silicon nitride also demonstrate a higher level of film integrity.

Vacuum CVD of silicon nitride has proven its quality impact, but in addition there is also a large potential cost reduction factor. It has been estimated that there is better than an 80% savings in operating cost over conventional atmospheric pressure CVD, and up to 99% savings in electrical power and gas consumption (5). This is even more important when considering today's concern over air pollution and energy shortages.

3.4.3 THE PROCESS FOR SILICON NITRIDE

The objective of this investigation was to apply the vacuum chemical vapor deposition of silicon nitride to solar cell fabrication. Also, since most of the previous work evolved empirically for equipment design and process control, this effort was directed toward a more theoretical analysis The analysis of chemical and gas kinetic theory provides possible explanations for observed process characteristics. Applying these theoretical assumptions, a deposition mechanism is suggested; it can be used as a criterion for determining process variables. This type of analysis should provide equipment and process design parameters for highly controllable vacuum chemical vapor deposited films.

3.4.3.1 PROCESS EQUIPMENT

The current equipment configuration of vacuum CVD systems has advanced quite rapidly since earlier laboratory systems. As in many production processes, success of vacuum CVD is directly dependent upon equipment development. As a major user, Motorola was a leader in the development of a production system which, during the last two years, has become the industry standard. Since silicon nitride deposition has been, historically, a difficult CVD process, the following discussion includes comments where equipment varies from that used for other CVD processes.

A schematic diagram of the system is shown in Figure 4. Typical of all current vacuum CVD systems is a cylindrical high temperature diffusion furnace element with three controllable temperature zones. The shorter end zones can be adjusted to provide a flat or linear temperature ramped profile along the center zone, depending on the desired CVD process. The temperature profile is adjusted by a set of calibrated thermocouples inserted into the diffusion furnace element. The control system can maintain $\pm 0.5^{\circ}C$ automatically. The reaction chamber is adapted to the vacuum system. An anodized aluminum end cap assembly, Figure 5, provides a vacuum seal to the quartz tube and reaction gas ports, and it also allows wafer loading access. Process gas control is provided by rotameter type flowmeters and needle-valve flow controllers mounted on the vacuum side of the flow meter, Figure 6. This configuration is required to be able to measure flows accurately. The process sequence is controlled by pneumatic valves operated by a computerized process timer. For very critical gas control or flow rate changes during the deposition, automatic mass flow controllers have been used. Mounted in the end cap assembly is a thermocouple (TC) type pressure sensor to provide process pressure monitoring. The pressure meter is mounted on the gas control panel and has switch contacts

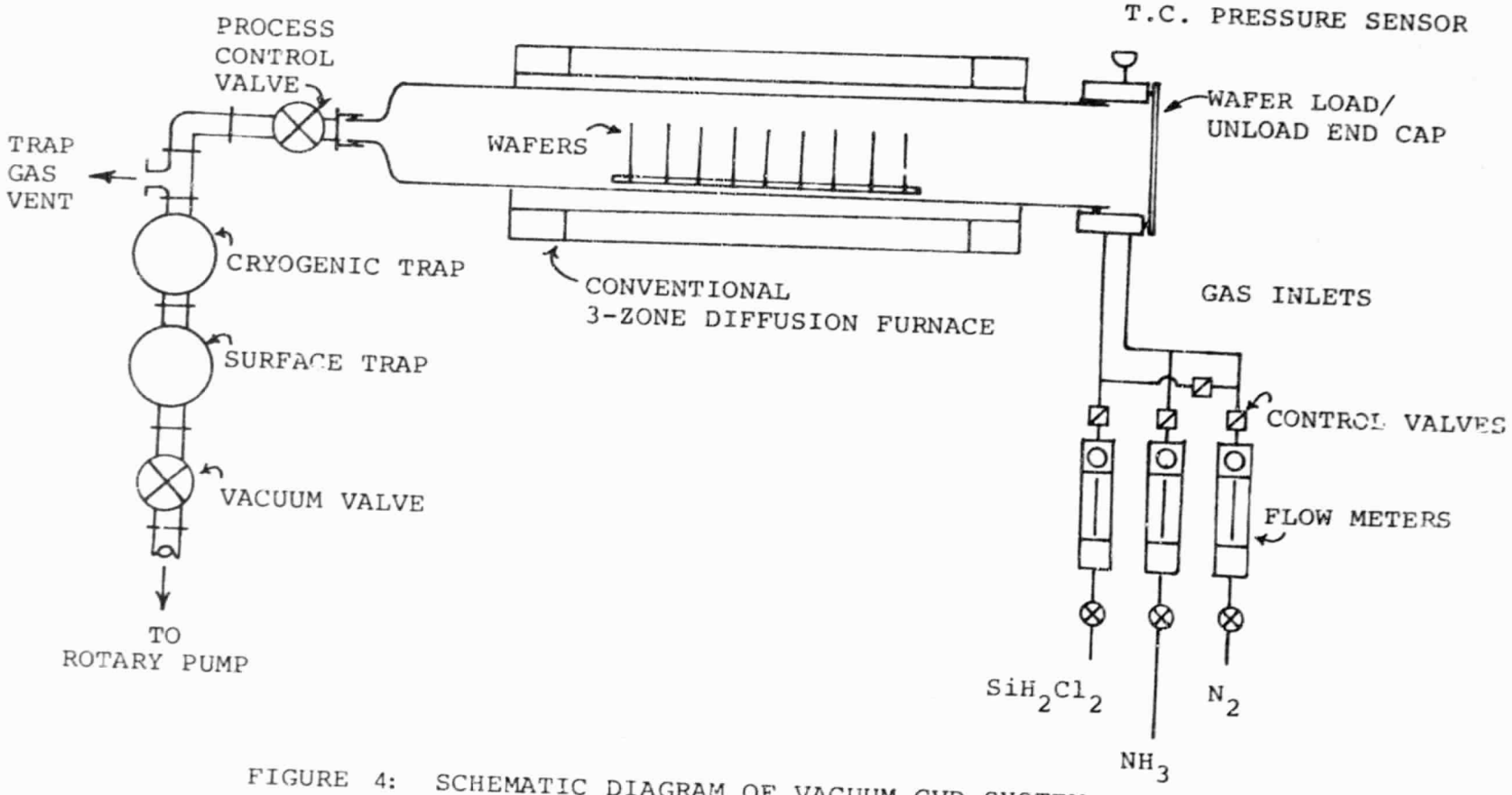


FIGURE 4: SCHEMATIC DIAGRAM OF VACUUM CVD SYSTEM FOR DEPOSITION OF SILICON NITRIDE.

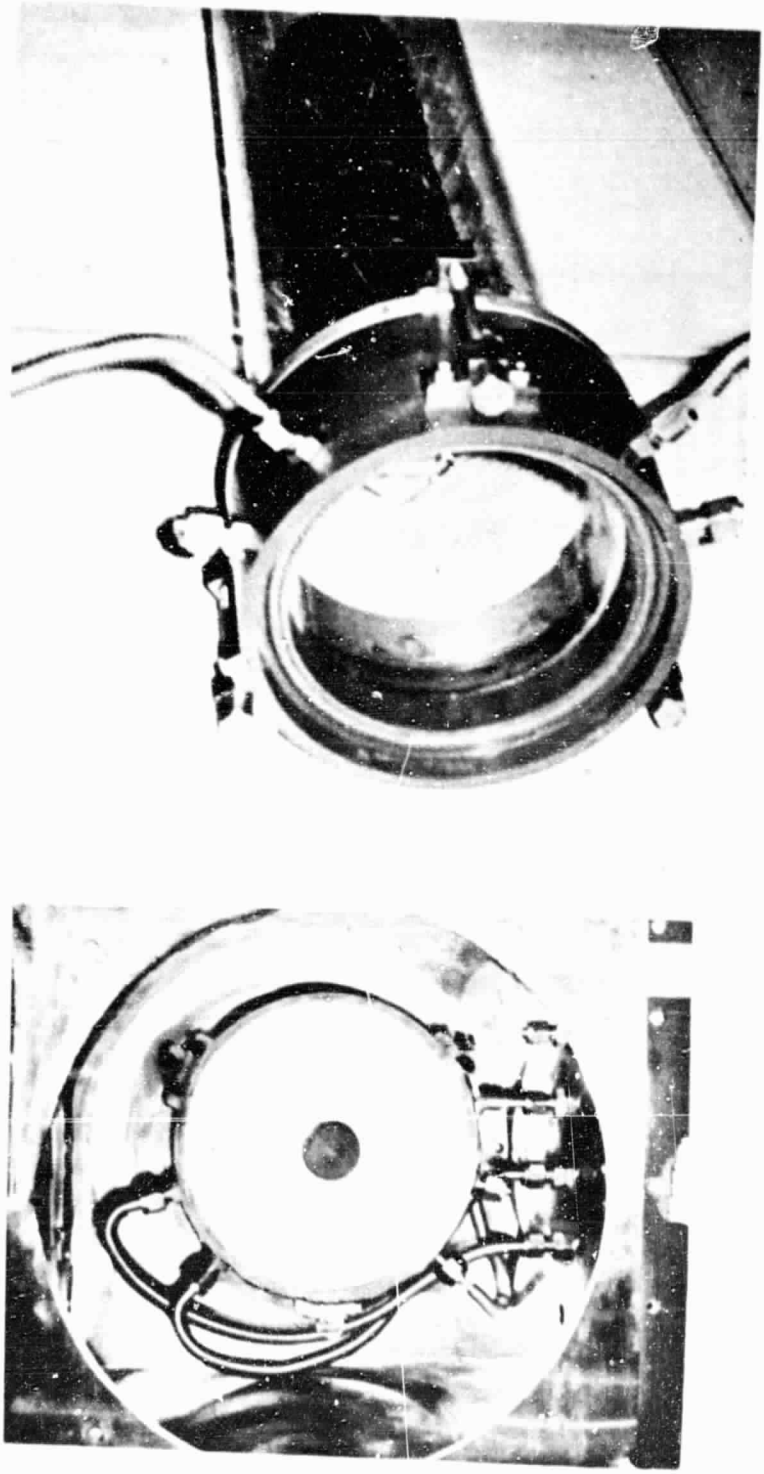


FIGURE 5: REACTOR TUBE END CAP ASSEMBLY. (BOTTOM PHOTO IS INSTALLED EQUIPMENT).

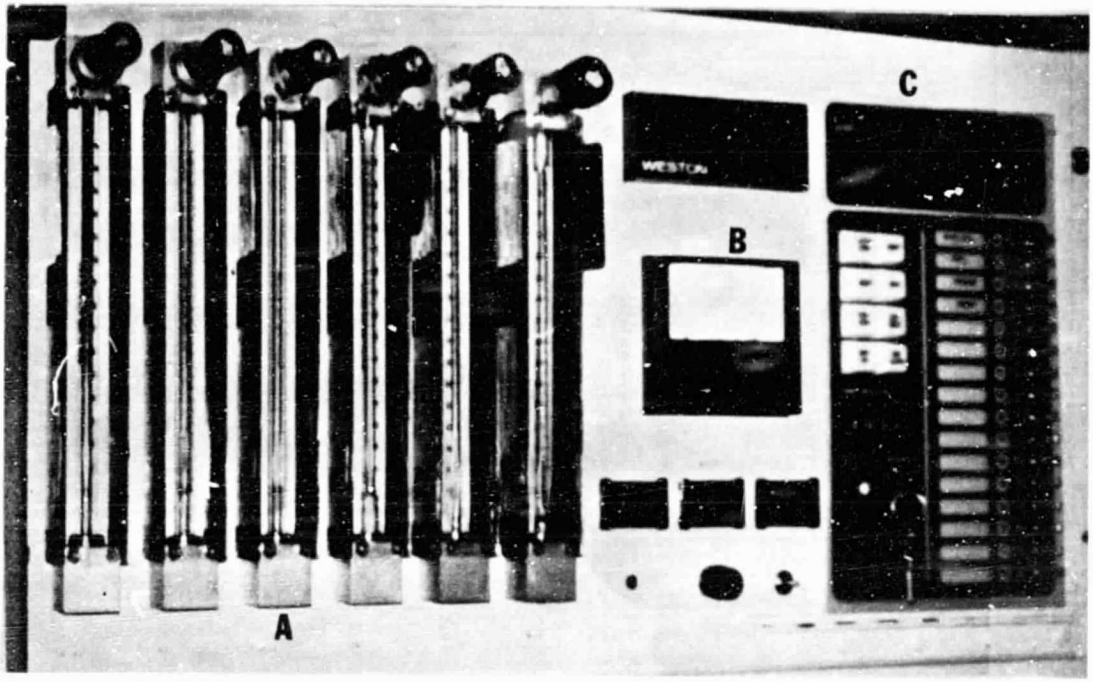
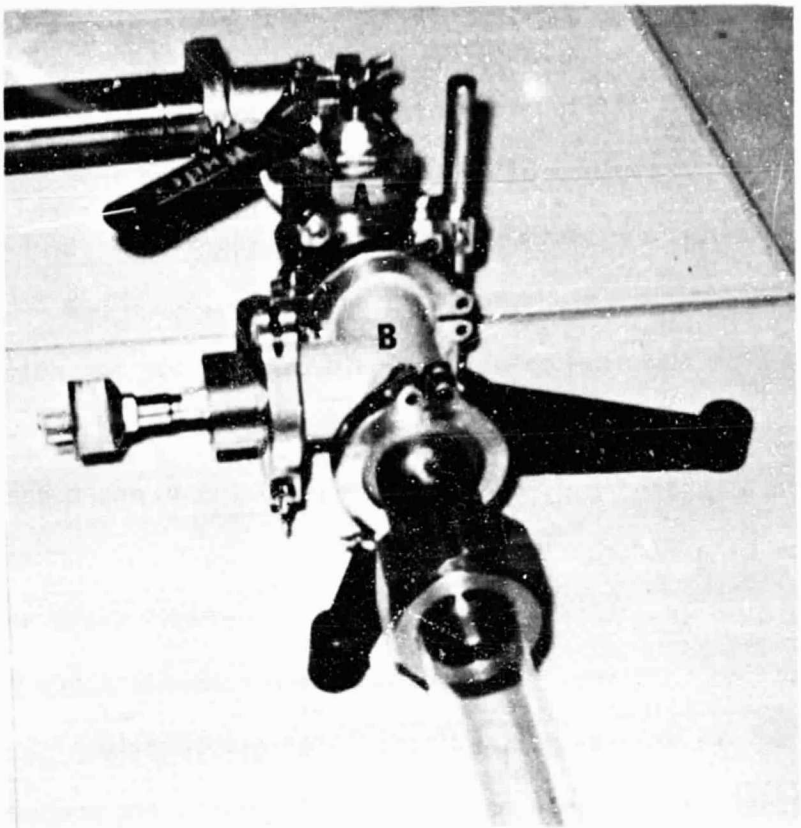


FIGURE 6: SYSTEM GAS PANEL WITH FLOW METERS (a), PRESSURE GAUGE, (b), AND PROCESS SEQUENCER (c).

used for safety shut off in event of vacuum failure. The front gas inlet is a departure from early laboratory systems which used a rear gas system available on the existing furnace system and discharged the product gases out the front end. (This configuration proved to be unsatisfactory since some reactant products, such as ammonium chloride, would contaminate the wafers during removal.)

The tube discharge end, Figure 7, is necked down and connected to the vacuum system by a compression O-ring fitting. Ball and socket joints and metal end caps are also used to provide a connection between the quartz tube and the vacuum system foreline. The vacuum system components are constructed of stainless steel to provide maximum life under exposure to high temperature corrosive gases. Also, since one of the major obstacles encountered was maintaining a leak free system, all connections are O-ring and flange type. This also allows for quick configuration changes and easier maintenance. The first vacuum component is a flow restriction valve which allows the use of a much smaller amount of gases than the vacuum pump's capacity. This allows adjustments in the working vacuum level to maintain process repeatability independent of pump speed fluctuations. It is the only system which allows gas flows and pressure to be varied independently. This feature provides a major improvement over earlier systems which were susceptible to fluctuations, or used expensive variable speed blowers to obtain the required control. Also, the earlier systems consumed five times the reactant gas, which significantly increased condensable product build-up on the vacuum components and in the pump.

The vacuum system components are shown in Figure 8. Since this process has both solid and condensable products, an automatically filled liquid nitrogen cryotrap is used. This condenses most of the harmful contaminants - ammonia,



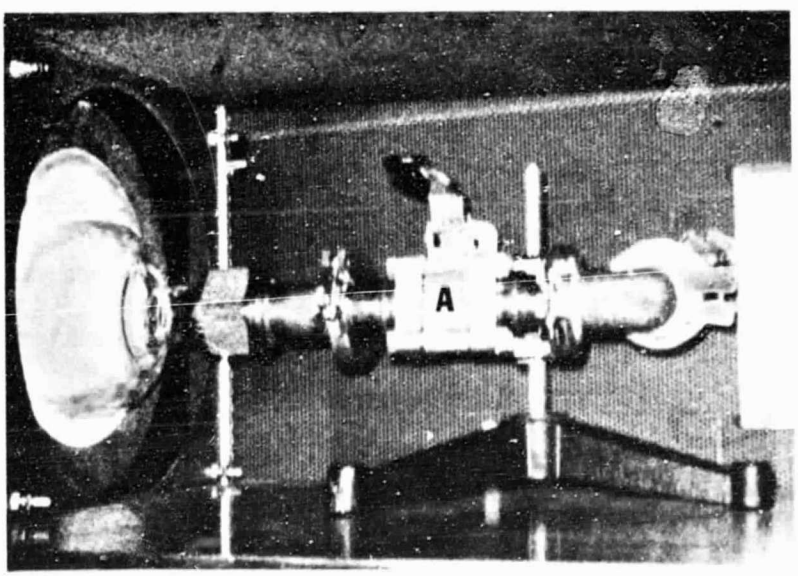


FIGURE 7: REACTOR TUBE DISCHARGE VACUUM CONNECTION WITH RESTRICTION VALVE (a), AND EXPERIMENTAL PRESSURE AND TEMPERATURE SENSOR TEE (b). (BOTTOM PHOTO IS INSTALLED EQUIPMENT.)

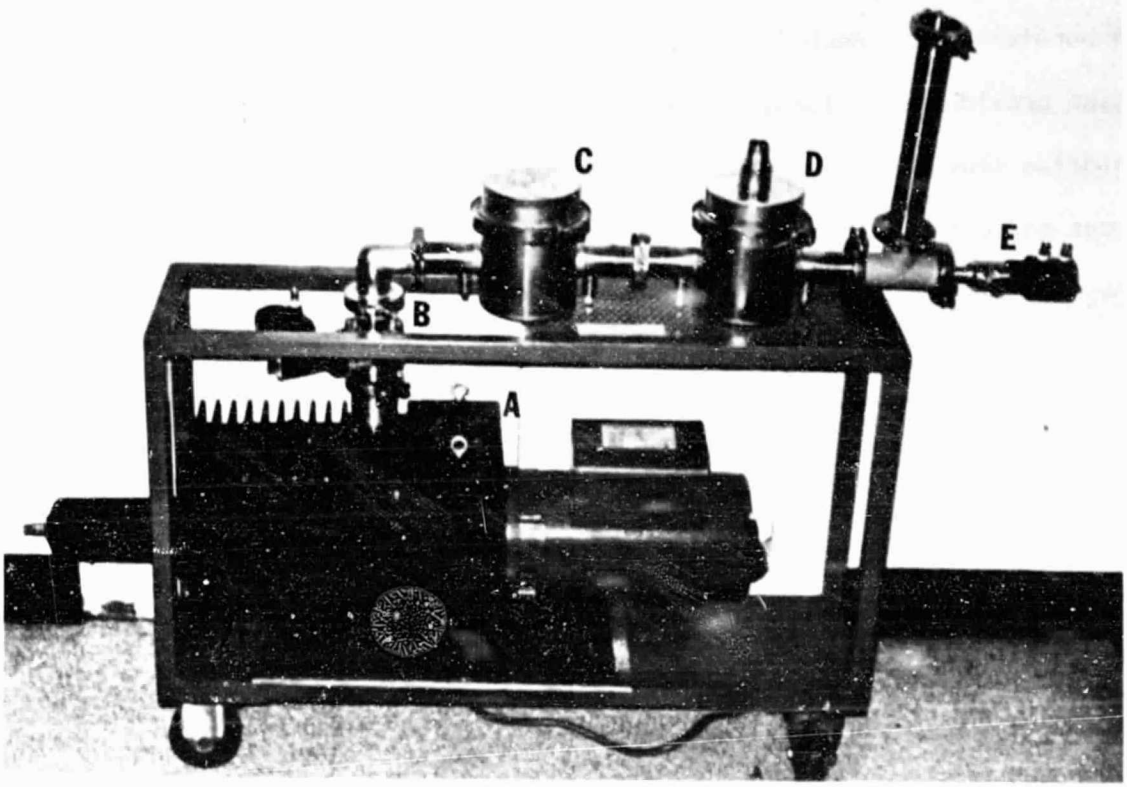


FIGURE 8 : SYSTEM VACUUM COMPONENTS WITH VACUUM PUMP (a), VACUUM VALVE (b), SURFACE TRAP (c), CYROGENIC TRAP (d), AND TRAP VENT VALVE (e).

ammonium chloride, and hydrochloride for the silicon nitride process. These would otherwise reduce the vacuum efficiency and destroy the pump's internal seals. Behind the cyrotrap is an exhaust valve and another TC pressure sensor. The exhaust removes product gas vapors from the trap as it increases to room temperature after deposition cycles. Next is a surface area trap or filter which provides additional condensation and blocks any loose particles of ammonium chloride from reaching the pump. Finally, a pneumatically operated vacuum valve opens and closes the system to the vacuum pump. The vacuum pump is a single-stage, chemical resistant unit; development of this direct drive, constant pumping speed unit was a major factor in the rapid development of the vacuum CVD process.

3.4.3.2 PROCESS DESCRIPTION

The thin films used for solar cell fabrication are normally deposited on silicon wafers of 2 to 4 inches in diameter (3 inch diameter is used in this report) and approximately 15 to 20 thousandths of an inch (mils) thick. The wafers are loaded vertically in a slotted quartz-rail boat. The wafer spacing is usually 3/16 inch due to industry standardization of handling and transport carriers. It should be noted that the spacing can have a significant effect on deposition, and will also have a major production cost impact. The wafers are identified by axial boat position starting from the inlet (load) end of the reactor tube. A majority of the process data are represented as thickness, or deposition rate, versus wafer axial position. To maintain process control, 3 to 5 wafers are evaluated after each deposition cycle. Data for this report were taken from a 150 wafer, 18 inch boat placed at the center of the reaction tube. Wafers in positions 2, 75, and 148 (and occasionally, 25 and 125) were

evaluated for thickness, index of refraction, and uniformity of the deposition. Also, all temperature measurements were made with a multi-thermocouple probe placed inside the reactor when it was at atmospheric pressure.

A typical deposition sequence consists of loading the wafer boat into the furnace tube and evacuating it to a pressure of 0.03 mm of Hg. A purge flow of nitrogen back fills the system to its operating pressure of 0.40 mm. During this operation, approximately 10 minutes, the wafer temperature is stabilized. Next the system is again evacuated to 0.03 mm and the ammonia gas flow is turned on; the system pressurizes to approximately the desired deposition pressure, and a final adjustment completes the cycle. Assuring an excess of ammonia at the start of deposition allows the reaction to start in a controlled manner. After 30 seconds, the dichlorosilane is injected, starting the deposition cycle which is usually 30 to 60 minutes long. This is optimized for a reasonable throughput while allowing moderately long time intervals for precise thickness control. At the completion of the deposition cycle, the dichlorosilane is turned off while the ammonia remains on for an additional 30 seconds to insure complete reaction. After the ammonia is turned off the system is evauated and purged with nitrogen. The vacuum valve closes and the system backfills with nitrogen to atmospheric pressure.

3.4.3.3 PROCESS OPERATION CHARACTERISTICS

Since the earlier systems, several important empirical performance characteristics have developed. The three most significant ones are the effect of axial deposition rates with increasing pressure and temperature, thickness uniformity versus operating pressure, and deposition rate as a function of wafer spacing. Similar generalized operation trends have been observed more or less for all CVD

processes, and form the basis for optimizing the silicon nitride system. Figure 9 is a generalized plot of the axial deposition rate versus temperature when all other variables are held constant. At higher temperatures and constant gas flow, deposition occurs more rapidly on the first wafers, depleting the reactants; thus, a decrease of deposition rate along the boat results. As the temperature is decreased, not only is the average deposition rate decreased, but the variation of the rate from wafer to wafer along the boat is decreased. A similar effect is noted if the pressure is varied with constant temperature and flow, Figure 10. At 2 mm, heavier deposition occurs on the first wafers, causing a reactant depletion that is too rapid. At sufficiently lower pressure, usually 0.5 to 0.4 mm, the axial uniformity of deposition rate is greatly improved.

The most significant trend noted is the effect of pressure variation upon film thickness uniformity across the wafer. As the pressure is reduced below 2.0 mm by either reducing gas flows or increasing exhaust rate, the thickness uniformity improves dramatically from a 20% variation to less than 1% at 0.4 mm pressure. This effect is illustrated in Figure 11.

Since the temperature-pressure uniformity effects are assumed to be related to reactant depletion along the boat, a similar effect is noted with closer wafer spacing or higher wafer density. Also, if wafer spacing decreases below a critical value, across-the-wafer uniformity is adversely effected. But, as the spacing decreases, average deposition rates increase. The wafer spacing effect is more reaction dependent than the other factors, and can greatly effect system operation. However, for the silicon nitride deposition process using dichlorosilane and ammonia, boat spacing variations normally seen, 3/8 to 3/32 inch, do not significantly change the deposition properties.

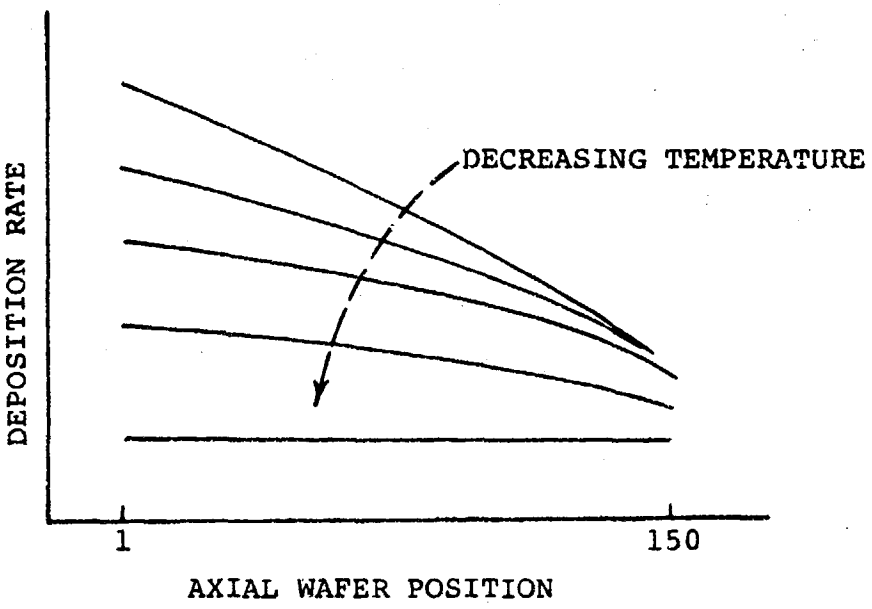


FIGURE 9: GENERAL TREND OF DEPOSITION RATE WITH DECREASING REACTOR TEMPERATURE, HOLDING ALL OTHER VARIABLES CONSTANT.

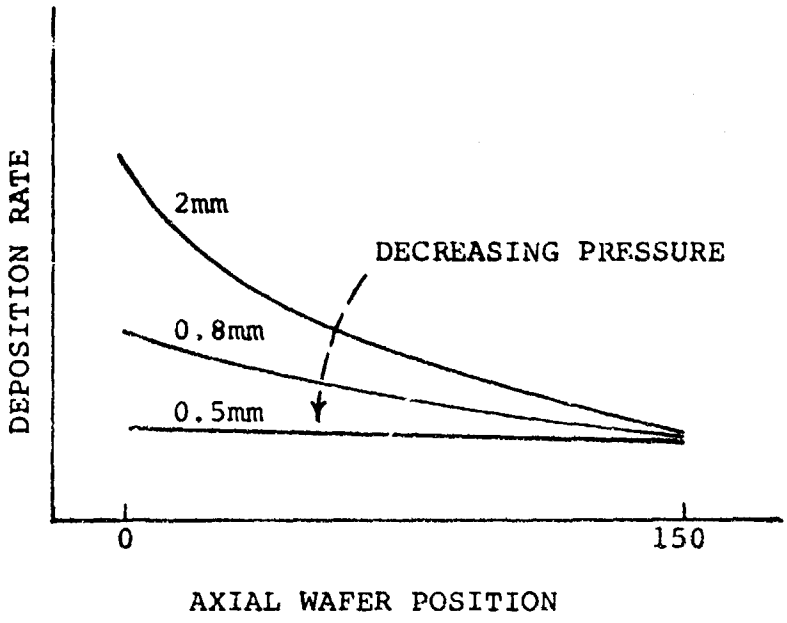


FIGURE 10: GENERAL TREND OF DEPOSITION RATE WITH DECREASING REACTANT FLOW RATE OR REACTOR PRESSURE, HOLDING REACTANT PARTIAL PRESSURES AND OTHER VARIABLES CONSTANT.

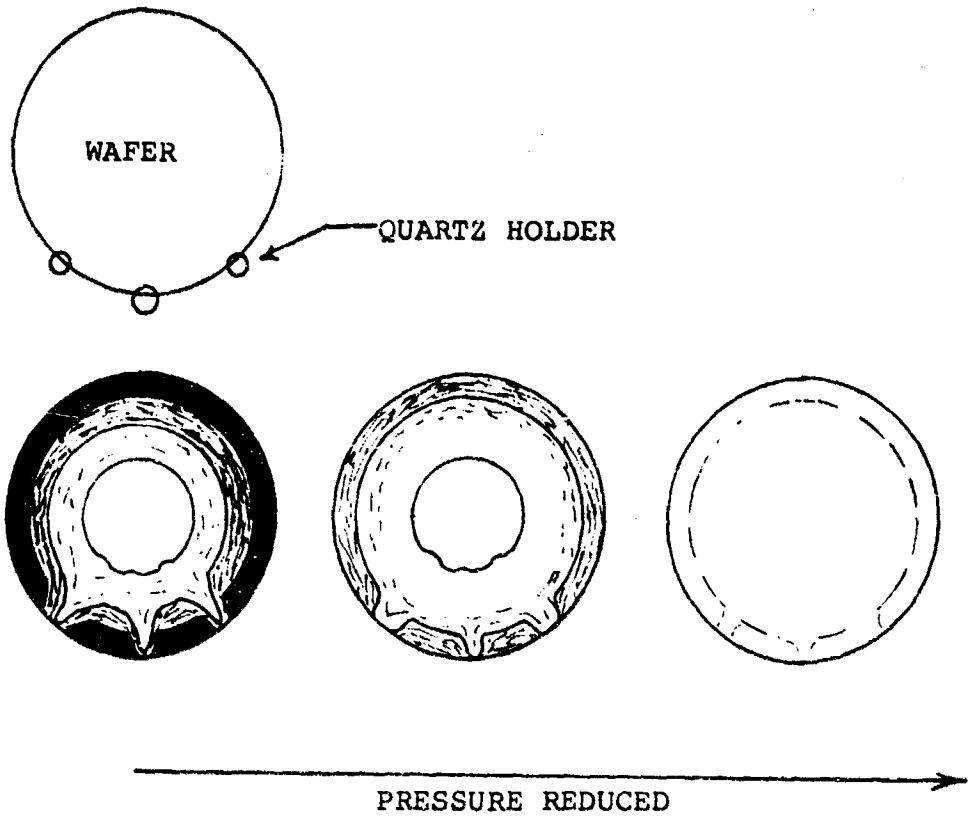


FIGURE 11: GENERAL TENDENCY OF THICKNESS UNIFORMITY ACROSS THE WAFER AS RELATED TO REACTOR VACUUM LEVEL. (DARKER TONES CORRESPOND TO THICKER DEPOSITION.)

The above general observations establish a method for optimizing the deposition process. An example of this procedure can be shown by assuming the required film is 750Å thick and must have maximum thickness uniformity across the wafer. For less than 2% thickness variation, an operating pressure less than 0.5 mm is selected. Due to manufacturing considerations, assume that 100 wafers per cycle per hour is desirable, so wafer spacing and gas depletion are not significant problems. A 20 minute deposition time at 0.4 mm may require 750°C temperature for a sufficient deposition rate. It should be noted, however, that the generalized characteristics are not completely independent; for example, a temperature of 750°C may cause a non-uniform deposition rate along the boat. So, as a normal procedure, the temperature at the inlet end is lowered, and that at the outlet end raised, usually 10° and 5°C respectively, to obtain uniform deposition. Experimental perturbations are repeated until the required results are obtained. This is an empirical process, and may not apply universally, e.g., to a new gas reaction. However, little theoretical discussion is available in the literature to develop a more adequate model. This problem is addressed later.

3.4.3.4 PROCESS RESULTS

When a system is optimized using the previous procedure, remarkable uniformity, cycle repeatability, and improved productivity can be realized over more conventional CVD systems using a horizontal RF reactor. On a routine basis for approximately 500 runs, this system produced wafers with a 1000Å film of silicon nitride with no detectable variation across the wafer surface. The index of refraction was 2.00 ± .01 for about 90% of the cycles. These measurements were taken using an AMS ellipsometer which has a thickness resolution of 10Å. Along the axial direction, repeatable deposition is easily

maintained within a ± 5% tolerance, with some cycles producing less than ± 1% variation. This uniformity can be compared favorably to that of a simple oxidation process in the same furnace system. Thus, it can be assumed that the control limitation is due mainly to furnace temperature and source gas stability.

3.4.4 PROCESS ANALYSIS

3.4.4.1 EXPERIMENTAL PROCEDURE

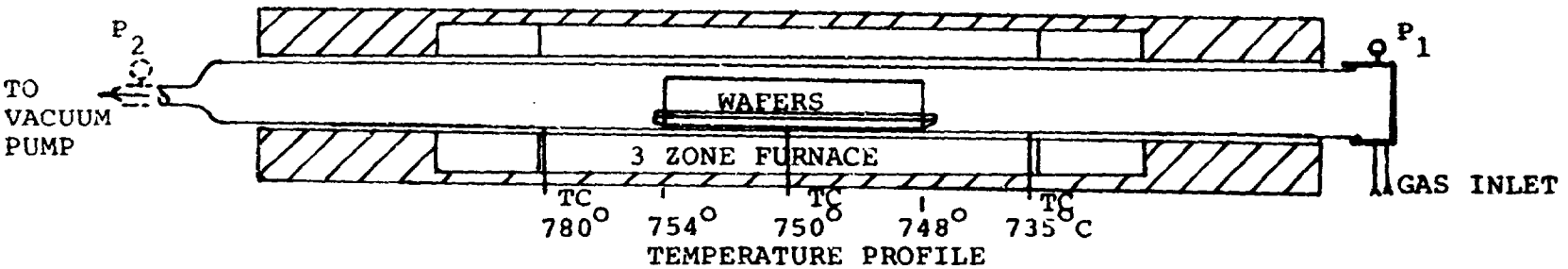
The data used in this report relate temperature, gas flow rates, pressure, and deposition parameters obtained during the development of a production process. A series of test deposition cycles using the process described in the previous section were run to determine the system operating characteristics. This repeated the results given in Tanikawa's work (3). Typical test data listed in Table 1 were used to establish process control and monitoring, and were also used in the discussion of kinetic theory in this report. The major system variables are temperature, reactant gas flow rates and ratio, and reaction pressure, which are related to deposition results--film thickness, uniformity and quality.

System temperature was adjusted by three thermocouples, installed in the furnace in the middle and at each end of the center zone as shown in Figure 12. These sense the reactor tube temperature for the control circuitry. They were adjusted by using a corresponding set of calibrated thermocouples placed in the reaction tube. Adjusting the end zones provided, along the reaction tube, a gradient temperature profile which was used to adjust the deposition rate along the boat. To determine actual wafer temperature, readings were taken with the thermocouples aligned to the position of the boat ends. Typical values used for the model process, listed on Figure 12, utilized a $6^{o}C$ ramp

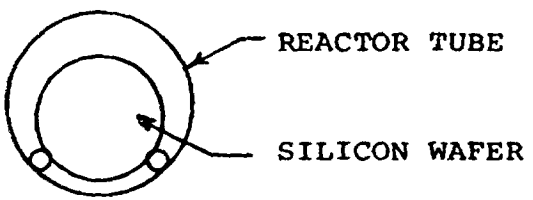
INLET GAS FLOW RATE N_2 (ℓ/s)	INLET PRESSURE P_1 (mm)	DISCHARGE PRESSURE P_2 (mm)	PRESSURE DROP ΔP (mm)	CALCULATED* PRESSURE DROP P_1-P_2 (mm)	DISCHARGE TEMPERATURE T_2 (°C)
1.0	0.38	0.26	0.12	0.108	87
1.3	0.43	0.30	0.13	0.140	89
2.0	0.56	0.34	0.22	0.216	90

*Values for Pressure Drop (P_1-P_2) were calculated using Poiseville Flow Equation.

TABLE 2 - GAS FLOW DATA -- MEASUREMENT OF INLET PRESSURE (P_1) DISCHARGE PRESSURE (P_2), AND DISCHARGE TEMPERATURE FOR DIFFERENT INLET NITROGEN FLOWS.



P_2 = 0.33mm
T_2 = 89°C



P_1 = 0.5mm
T_1 = 27°C
$\dot{v}_1$ = 1.27 ℓ/s
V_1 = 14.5cm/s
Ammonia
$\dot{v}_o$ = 32.5cc/min
Dichlorosilane
$\dot{v}_o$ = 11.8cc/min

FIGURE 12: MODEL PROCESS DATA FOR REACTOR TEMPERATURE PROFILE.

along the length of the wafer carrier. Temperature adjustment was the major method of maintaining axial deposition uniformity.

Reactant gas flows were metered by manually adjusted microflow needle valves. The flow was measured by Brooks low flow 150 mm rotameters. The flow meter readings were converted to flow rates using manufacturer's calibration data.

Reaction pressure was monitored at the end cap using a thermocouple vacuum gauge. This type of gauge operates by sensing the temperature effect of pressure on a wire heated by a constant current. Although very dependent on molecular weight and heat capacities of the gas, it does provide accurate readings of many dissimilar gases from 0.3 to 0.8 mm. The effect of pressure reduction was most noticeable on wafer surface uniformity as illustrated earlier in Figure 11. For constant gas flows, the pressure was adjusted by a restriction valve. As a result of this experimentation, a pressure between 0.4 and 0.5 mm was found best suited for uniform deposition of silicon nitride; this is lower than that utilized in other commercial processes (6).

After evaluation of data from the above procedure, it was determined that additional data not obtained from normal equipment configuration was required. Information was needed to solve the closed system gas model for the flow kinetics, requiring knowledge of two of the four gas flow variables--temperature, pressure, velocity, and mass flow rate--at the reaction tube discharge end. Temperature and pressure were determined to be easier to measure. Nitrogen was used as a flow medium to eliminate reaction density changes, heat capacity effects on the pressure readings, and reaction deposits on the thermocouple. A pressure thermocouple sensor was installed in a tee section of the discharge line ahead of the restriction valve (as shown earlier in Figure 7). The discharge pressure was read with the same equipment as the inlet pressure. A calculation of pressure change due to area reduction from the reaction tube and discharge line

gave less than 0.01 mm difference. Since this was less than the instrumentation accuracy, readings in the discharge line were taken as the reactor tube exit pressure. Values of the inlet and discharge pressures for different flows are listed in Table 2 with calculated values from the Poiseville equation for viscous flow in a long cylindrical duct. A temperature thermocouple was then installed in the center of the discharge line. To reduce cooling effects, the discharge line was heated to 120°C by venting high gas flow through the reaction tube. The system was evacuated, and with a nitrogen inlet flow of 1.2 ℓ/sec. at 0.5 mm, the discharge temperature was measured as 89°C and remained stable. Similar results were obtained at different pressures, Table 2.

The deposited film thickness and index of refraction were measured simultaneously on an AME-500 Ellipsometer. The ellipsometer produces a beam of elliptically polarized light. The thickness and refractive optical properties of thin transparent films can be determined by measuring the change in ellipticity and polarized angle of the reflected beam. For a silicon nitride film less than 1300Å, the ellipsometer has an accuracy of ±3Å for thickness and ±0.005 for index of refraction. In the test deposition cycles, the fifth wafer was also evaluated (besides the three used for process control data). These measurements were used to obtain temperature dependence of the reaction without reactant depletion effects.

3.4.4.2 THEORETICAL DISCUSSION

3.4.4.2.1 LITERATURE REVIEW

In the more pertinent articles on the low pressure dichlorosilane process, there is a general lack of theoretical discussion from which a deposition model can be developed (3,6). In fact, an analysis of some gas kinetic

parameters seems to be in conflict with earlier proposals of turbulent gas flow between the wafers which aids in deposition uniformity (3). An extensive review of literature on related CVD processes was completed to obtain a more thorough background. Most of the available data are based on the horizontal atmospheric reactors or single substrate laboratory systems. Considerable research has been done on horizontal RF reactors, since they have been the mainstay of CVD processing for over 10 years. Also, due to the cold reactor wall and the spacing of the RF induction coils, both systems are easily accessible to in situ analysis. This has facilitated extensive characterization of these system's temperature profiles, gas chemical composition, and flow dynamics (7), although for different chemical reactions and equipment configurations, reported work did provide some insight and assumptions needed to develop a deposition mechanism theory for the low pressure process. Several research papers describe laboratory systems using a single wafer induction heated susceptor (8, 9, 10). In most cases, this equipment uses a high flow nozzle normal to the substrate surface and operates in the pressure range from one half to one atmosphere. Considerable theoretical discussion of possible deposition mechanisms usually predicts a diffusion rate-limiting process at higher temperatures. This is the case for most heated susceptor deposition models developed to date. In the investigation of silicon nitride deposition using a silane-hydrazine process, Yoshioka and Shigetoshi found (5) that the Arrehenius temperature relationship suggested two kinetic mechanisms. Above 750°C, an approximately saturated deposition rate was interpreted as a mass transport limitation. But between 550°C and 650°C, an activation energy of 54 kcal/mole was assumed to be a chemical reaction rate limitation. This is approximately the energy required to break the nitrogen bond of the hydrazine molecule in the following reaction:

$$N_2H \rightarrow 2\ NH_2, \Delta G^{\circ} = 60\ kcal$$

They also suggested a possible transition-state reaction theory where the activated complex is polymerized silicam [$(SiN)_2NF$] molecules formed from silicon diimide [$Si(NH_2)_2$]:

$$3\ Si(NH_2) \rightarrow (SiN)_2NH + NH_3$$

$$3\ (SiN)_2NH \rightarrow 2\ Si_3N_4 + NH_3$$

A similar reaction mechanism was proposed by Chu, Lee, and Gruber (11) using the silicon tetrachloride and ammonia reaction, based on the chemical reaction first proposed by Max Blix (12) for the polymerization of silicon diimide complexes.

Effects of gas flow patterns and mass transfer of reactants in the gas phase frequently control deposition rates. A Hitachi research group performed a detailed study of the horizontal reactor (13). They used a resistance heated susceptor and $TiCl_2$ flow visualization techniques. At lower flow rates, they discovered and modeled a complex vortex flow pattern due to a combination of free and forced convection heating over the hot susceptor. This demonstrated the uniformity problems characteristic of the horizontal reactor. At higher flow rates used to obtain pure forced convection laminar flow, they showed the existence of a zero flow velocity (stagnant) layer. This verified the reactant diffusion rate limitation model developed for this deposition technique at higher temperatures. Of interest to vacuum CVD were their observations that below atmospheric pressure (160 torr) all vortex motion stopped and the flow became viscous streamliners. This was the easiest way to obtain the desired laminar flow without free convection effects; but due to visualization and equipment limitations, lower pressures were not studied further.

Similar studies for the horizontal reactor have centered about the very important process for deposition of silicon by pyrolysis of silane (SiH_4) and chlorosilanes. Vladimir Ban (14, 15) has reported several significant

results for the horizontal reactor kinetics and chemical decomposition of dichlorosilane. Using sensitive microscopic mass spectrometry and temperature measurement techniques, he was able to study the actual process in great detail. He verified the Hitachi research and even measured the thickness of the stagnation layer for various conditions. Of particular interest are his observations at higher flow velocities where the gas temperature 2 cm above the 1000°C susceptor was below 300°C near the exhaust end. Also, in his chemical analysis for pyrolysis of silicon from dichlorosilane, he found considerable indication of intermittent reactant species, predominantly silicone dichloride ($SiCl_2$) conforming to the following stoichiometric equations:

$$SiH_2Cl_2 \xrightarrow{HCl} SiCl_2 + H_2$$

$$SiCl_2 + H_2 \longrightarrow Si + 2\ HCl$$

This was found to be the situation even though $SiCl_2$ is less stable than SiH_2Cl_2 below 1200°K. He also theorized that the decomposition of silicon dichloride became the rate-limiting mechanism at lower temperature and excess hydrogen chloride conditions.

In a detailed theoretical discussion of the CVD of silicon by silane pyrolysis, Ananda Prature (16) described the possible heterogenous kinetic mechanisms. These include mass transport of the reactant (silane) to the surface, absorption at the surface, surface reaction, and the desorption of a gaseous product (hydrogen). Besides developing equilibrium rate equations for the above mechanisms, he also reviewed various current experimental results to relate these to possible rate-limited reactions. As previously mentioned, mass transport can be limited by reactant diffusion through the stagnant layer in an atmospheric pressure system at higher temperatures. At lower temperatures, there is general agreement that one (or a combination) of chemisorption, surface reaction, and product desorption is the limiting step. To evaluate the rate equations presented by Praturi, independent data are needed for each

species absorption constant and detailed chemical reaction mechanism.

From this review, it became apparent that further investigation of flow kinetics at lower pressures was needed to evaluate mass transport of reactants. Also, identification of possible intermittent complex reactions and study of physical absorption would be required to discuss a deposition model.

3.4.4.2.2 GAS KINETICS

As related by several authors in the literature review, mass transport can be the primary rate-limiting factor. Introduction of the low pressure system to a known process caused such significant changes that any analysis of a deposition model must first include a complete study and characterization of the system's gas dynamics. Furthermore, most of the variables required for further analysis of chemical kinetics are defined in terms of the gas dynamics or measured system parameters such as flow rates, temperature, and pressure.

Each parameter must be defined in a general expression, and then calculated values given for the numerical example discussed in detail. This is done here for the closed system model illustrated in Figure 12 with the example process data listed. Inlet gas flows were determined by rotometer flow measurements with needle type adjustable orfice flow control valves. The flow meters were placed before the control valves in order to give accurate measurement. With proper setting of the vacuum level, this simple system provided adequate control. With low regulated pressures (1 to 3 psi), the inlet gases were at approximately standard conditions at the flow meters (≈ 1% error at 3 psi) but undergo more than a 1500:1 expansion to 0.5 mm. The first calculation was the gas law equation relating gas inlet volumes and densities to those in the reaction chamber. Densities are related by:

$$\rho_1 = \frac{P_1}{P_A} \rho_o$$

ρ_o = density at atmospheric pressure (g/cm^3)

ρ_1 = density of inlet gas (g/cm^3)

P_A = atmospheric pressure (mm of mercury)

P_1 = system inlet pressure (mm of mercury)

Volume expansion is given for the volume rates by:

$$\upsilon_1^o = \frac{P_o}{P_1} \upsilon_o^o$$

υ_o^o = measured volume flow rates (cc/min)

υ_1^o = inlet volume flow rate (cc/min)

P_o = supply pressure (mm)

The flow meter reading (mm) is converted to units of cc/min using manufacturers' calibrated charts for air, and converting to the given gas using the specific gas ratio. Also, the mass flow rate is similarly defined as:

$$\dot{m}_1^o = \rho \upsilon_1^o$$

$\dot{m}_1^o$ = inlet mass flow rates (g/sec)

Example flow rate for the model process for nitrogen is:

$\rho_o = 1.165 \times 10^{-3}$ g/ℓ (17)

$\rho_1 = \left(\frac{0.5mm}{760mm}\right) (1.165 \times 10^{-3}$ g/ℓ$) = 7.664 \times 10^{-7}$ g/ℓ

$\upsilon_o^o = 46$ cc/min $= 7.67 \times 10^{-4}$ ℓ/s at 2 psi

$\upsilon_1^o = \left(\frac{860mm}{0.5mm}\right) (7.67 \times 10^{-4}$ ℓ/s$) = 1.382$ ℓ/s

$\dot{m}_1^o = \rho \upsilon_1^o = 8.98 \times 10^{-7}$ g/s

for ammonia (18):

$\rho_o = 0.7188$ g/ℓ $\rho_1 = 4.179 \times 10^{-4}$ g/ℓ

$\upsilon_o^o = 32.5$ cc/min. $\upsilon_1^o = 0.932$ ℓ/s

$\dot{m}_1^o = 3.893 \times 10^{-4}$ g/s

for dichlorosilane (18):

$\rho_o = 4.168$ g/ℓ $\rho_1 = 2.423 \times 10^{-3}$ g/ℓ

$\overset{o}{v}_o = 11.77$ cc/min $\overset{o}{v}_1 = 0.337$ ℓ/s

$\overset{o}{m}_1 = 8.176 \times 10^{-4}$ g/s

also, the combined density is 7.043×10^{-4} g/ℓ.

The next important parameter was the inlet gas molar ratio required for any discussion of chemical or thermodynamic reaction properties. The mole fraction is defined as (18):

n_i = number of moles of i^{th} component

x_i = mole fraction of i^{th} component

$$x_i = \frac{n_i}{n_{TOT}}$$

The number of moles of the reaction gases can be determined from mass flow rates and atomic weights:

ammonia: $M = 17.09$ g/mol

$$\overset{o}{n} = \frac{\overset{o}{m}}{M} = \frac{3.893 \times 10^{-4} \text{ g/s}}{17.03 \text{ g/mol}}$$

$$\overset{o}{n} = 2.286 \times 10^{-5} \text{ mol/s}$$

dichlorosilane: $M = 101.1$ g/mol

$$\overset{o}{n} = 8.087 \times 10^{-6} \text{ mol/s}$$

So the molar ratios are:

ammonia:
$$x = \frac{2.286 \times 10^{-5} \text{ mol/s}}{3.095 \times 10^{-5} \text{ mol/s}}$$

$$x = 0.739$$

dichlorosilane: $x = 0.261$

which is about 1 mole of dichlorosilane to 6 moles of ammonia.

For gas reactions, concentration of species is normally defined as a function of partial pressure by Dalton's Law of Partial Pressure where (19):

$$p_i = X_i \, P_{TOTAL}$$

p_i = partial pressure of i^{th} component (mm)

x_i = molar fraction

so for ammonia:

$p = (0.739)\ (0.5\ mm)$

$p = 0.369$

and for dichlorosilane: $p = 0.131$ mm.

The previous calculations have only related measured values to those of the reactants at the reaction inlet and have not described any kinetic properties of the system. Next, the system must be classified as to the type of flow before the proper gas dynamic equations can be applied. Since classification, and also possibly some chemical kinetics, are dependent upon gas collision theory, the collision properties must be evaluated next.

Molecular collision diameter, σ, is a basic property of the gas and is used to determine other properties. From available experimental data (20), the nominal collision diameter for ammonia is 4.340Å (1Å = 10^{-8}cm). However, there are no reliable data available for dichlorosilane, so an estimation technique is used. The collision diameter estimation equation is given as (20):

$$\sigma = [2.3351 - 0.087\ \omega] \left(\frac{T_C}{T}\right)^{1/2}$$

where

σ = collision diameter (Å)

ω = eccentric factor (or nonsphericity)

T_C = critical temperature (highest temperature for separated gas and liquid phases)

also $\omega \approx \frac{3}{7}\left(\frac{\Theta}{1-\Theta}\right) \log P_C - 1$

$\Theta = \frac{T_b}{T_c}$

T_b = boiling temperature

P_C = critical pressure.

The collision diameter, σ, calculates to be 4.992Å for dichlorosilane, which

appears reasonable since available data for silicon tetrafluoride give a value of 4.880Å (20).

The previous properties describe static, equilibrium state molecular properties such as density and pressure, whereas, viscosity is a dynamic, nonequilibrium macro system property. Thus, it is used to correlate static state properties to those of a dynamic system. Viscosity is a measure of internal friction which tends to oppose dynamic change in the system motion; therefore, it determines the fluid velocity as a function of the systems physical characteristics. This can be numerically used to classify the fluid system for which transport properties have been studied. Since viscosity is a function of temperature, relationships were found to evaluate gas viscosity and its temperature dependence. Normally, viscosity is independent of pressure, but when the pressure is reduced below 1 mm some adjustment must be included (20).

For the low pressure range, viscosity for ammonia has been measured experimentally as (20):

μ (μP)	T (^{o}C)
90	0
131	100
151	400

An estimation technique has been developed empirically for low pressure, hydrogen-type bonded polar molecules, i.e. ammonia, which verifies this experimental data and provides a temperature dependence equation (21):

$$\mu = \frac{(0.755\ T_r - 0.055)\ Z_c^{-5/4}}{T_c^{1/6}\ M^{-1/2}\ P_c^{-2/3}}$$

where Z_c = critical point compressibility factor

T_r = reduced temperature

T_c = critical temperature

P_c = critical pressure

M_i = atomic mass.

A similar estimation equation was used to obtain values for the temperature dependence of dichlorosilane. No reliable data were found for dichlorosilane, so all values for viscosity are based on this estimation technique. In the low pressure range, the semi-empirical equation is given as (20):

$$\mu = \frac{a^* T_r}{[1 + 0.36\, T_r (T_r - 1)]^{1/6}}$$

$$\text{where } a^* = \frac{3.5 M^{1/2} P_c^{2/3}}{T_c^{1/6}}$$

so at the operating inlet pressure, and (probable) temperature of 100°C, the estimated value is 137μP or 1.37×10^{-4} g cm^{-1} s^{-1}. Since this equation usually has a ± 3% accuracy, and the experimental viscosity of silicon tetrafluoride is 146.7μP, the estimated value is probably a reasonably number.

It should be noted that the viscosity of gas mixtures is seldom a linear combination, and can greatly exceed either pure gas value. Since this is particularly true for ammonia binary gas mixtures, the combined viscosity of the ammonia - dichlorosilane system was estimated to ensure a more accurate value. For a low pressure binary gas system, the viscosity is given by (20):

$$\mu_{mix} = \frac{X_1 \mu_1}{X_1 + X_2 \phi 12} + \frac{X_2 \mu_2}{X_2 + X_1 \phi_2}$$

where X_1, X_2 = molar fractions

μ_1, μ_2 = pure-component viscosities

ϕ_{12}, ϕ_{21} = ratio parameters

$$\phi_{12} = \frac{\left[1+(\mu_1,\mu_2)^{1/2}(M_2/M_1)^{1/4}\right]^2}{\left\{8\left[1+(m_1/M_2)\right]\right\}^{1/2}}$$

$$\phi_{21} = \phi_{12}\frac{\mu_2}{\mu_1}\frac{M_1}{M_2} .$$

For a dichlorosilane and ammonia mixture, the binary gas viscosity was found to be 139.1μP at 100°C. Although not a very significant increase over the estimated dichlorosilane value, it was used in following calculations as the viscosity value.

The mean free path of the gas system is one of the most important properties; it ultimately relates to other parameters such as coefficient of viscosity, heat conductivity, diffusivity, and collision frequency. So, for a molecule in a binary gas mixture, the mean free path L_1 of the ammonia molecules is given by (19):

$$\frac{1}{L_1} = \sqrt{2}\pi n_1 \sigma_1^2 + \pi n_1 \sigma_{12}^2 \left[1+\frac{M_2}{M_1}\right]^{1/2}$$

Using the following values, L_1 calculates to be:

$L_1 = 4.795 \times 10^{-3}$ cm

n = number of molecules per cubic centimeter

$= 9.656 \times 10^{18} \frac{Pmm}{T}$ cm^{-3}

$n_1 = 9.504 \times 10^{15}$ cm^{-3} (ammonia)

$n_2 = 3.373 \times 10^{15}$ cm^{-3} (dichlorosilane)

$\sigma_1 = 4.340$Å

$\sigma_2 = 4.992$Å

$\sigma_{12} = \frac{1}{2}(\sigma_1 + \sigma_2) = 4.666$Å

$T = 100$°C

From equations above, it is noted that the mean free path is directly proportional to temperature and inversely to pressure. The above relationships are for static gases and do not include mean gas flow effects; but more important, they do not include container wall effects. Where the dimensions of the system begin to approach the order of a mean free path for gas molecules, there is a significant effect of wall collisions that increase the mean free path between gas molecule collisions by a factor of two (21). This condition can exist between the vertically spaced wafers.

Related to mean free path is the number of collisions between molecules per unit time, which is usually related to the chemical kinetics. For a binary gas system, the number of collisions between ammonia and dichlorosilane (unlike) molecules is expressed as (19):

$$Z_{12} = 4.571 \times 10^{4}\, n_1 n_2 \sigma_{12}^{2}\, [T(\frac{1}{M_1} + \frac{2}{M_2})]^{1/2}$$

$$Z_{12} = 1.614 \times 10^{22}\ cm^{-3}s^{-1}$$

compared to the number of collisions between ammonia (like) molecules:

$$Z_{11} = (3.232 \times 10^{4})\, n_1^{2} \sigma_1^{2}\, (\frac{T}{M})^{1/2}\ cm^{-3}s^{-1}$$

$$Z_{11} = 2.573 \times 10^{22}\ cm^{-3}s^{-1}$$

and for dichlorosilane molecules:

$$Z_{22} = 9.223 \times 10^{20}\ cm^{-3}s^{-1}.$$

Also of interest is the rate at which gas molecules strike a surface, since the absorption of molecules on a surface is dependent upon the collision transport property. For ammonia molecules, the collision rate with a surface is expressed as (19):

$$\nu = 3.513 \times 10^{22}\ \frac{Pmm}{(MT)^{1/2}}\ cm^{-2}s^{-1}$$

$$\nu = 3.253 \times 10^{20}\ cm^{-2}s^{-1}$$

and for dichlorosilane:

$$\nu = 2.369 \times 10^{19} \text{ cm}^{-2}\text{s}^{-1} \quad .$$

The previous section described the molecular transport parameters, for the most part, for a fluid system at rest. Using these developed parameters, some discussion can now be made concerning the flow mechanism of the dynamic, macro system. Using the definition of Knudsen number which delineates the ranges of viscous, transitional, and molecular flow (19), the system can be defined as viscous flow since

$$\frac{L_{av}}{a} < 0.01 \text{ for viscous flow.}$$

where L_{av} = average pressure mean free path

a = characteristic system dimension.

For a reaction tube radius of 5 cm, the Knudsen number is:

$$\frac{L_{av}}{a} \approx \frac{5.5 \times 10^{-3} \text{cm}}{5 \text{ cm}} \approx 1.1 \times 10^{-3} < 0.01.$$

As shown later, the spacing between wafers can change this viscous assumption, since it is of the order of 0.25 cm and for close parallel plates,

$$\frac{L_{av}}{a} \approx \frac{2L}{a} \approx 0.05$$

which is within a transition flow range and could easily become molecular flow.

The gas flow rate can be used to determine the mean flow velocity in the reaction tube. Assuming an average pressure of 0.45 mm and using the inlet volume rate, the flow rate, Q, is found to be 1.21 $\ell.\text{mm}.\text{s}^{-1}$, where Q is related to flow velocity by (19):

$$V = \frac{Q}{A}$$

where V = flow velocity, cm s^{-1}

$$= \frac{1.21 \times 10^{3} \text{ cm}^{3}.\text{s}^{-2}}{86.6 \text{ cm}^{2}}$$

$$V = 13.972 \text{ cm s}^{-1}$$

This also yields the mean residence time; an estimate of the time a gas molecule will remain in a 200 cm long reaction tube is approximately 16 seconds.

Another measure of the flow mechanism is normally related to the dimensionless flow quantity known as the Reynolds number which delineates viscous and turbulent flows. For a circular cross sectional tube the Reynolds number is defined as (22,23):

$$Re = \frac{a\ \rho\ Vav}{\mu}$$

where a = radius, cm

ρ = density, g cm^{-3}

Vav = average flow velocity, cm s^{-1}

μ = coefficient of viscosity, g $cm^{-2} s^{-1}$

so

$$Re = \frac{(5.05)(7.043 \times 10^{-7})(13.97)}{(1.391 \times 10^{-4})}$$

$$Re = 0.36$$

Since a Reynolds number below 2000 defines laminar flow, there should be little turbulence in the flow even considering non ideal inlet conditions. This, compared to the horizontal wafer RF reactor (at atmospheric pressure) is a reduction of two orders of magnitude.

For a viscous, laminar flow in a long tube, the Poiseville flow equation should define the system pressure. Assuming a suction (negative pressure) flow, the Poiseville equation can be written as (19):

$$P_1 - P_2 = \frac{8\mu\ell\ Vav}{a^2}$$

where P_1 = inlet pressure, mm

P_2 = outlet pressure, mm

ℓ = tube length, cm

Vav = average velocity, cm s^{-1}

a = tube diameter, cm

μ = coefficient of viscosity, g $cm^{-1}s^{-1}$

so

$$P_1-P_2 = \frac{8(1.391 \times 10^{-4} \text{ g cm}^{-1}\text{s}^{-1})(210 \text{ cm})(13.97 \text{ cms}^{-1})(1.359\text{mm cm}^2\text{gs}^2)}{(5.05 \text{ cm})^2}$$

$$P_1-P_2 = 0.174 \text{ mm}$$

so,

$$P_2 = 0.5 \text{ mm} - 0.174 \text{ mm}$$

$$= 0.326 \text{ mm}$$

The only remaining significant parameter is the gas temperature as a function of axial position. From experience, the exhaust temperature was not unreasonable; in fact the exhaust line had to be insulated on occasion to maintain temperature above the condensation point of ammonium chloride. Several gas flow analysis models were tried, but due to the molecular heat transfer at these low pressures, they did not provide reasonable results (22, 23, 24, 25). To estimate the temperature relation and to verify other conclusions, addition measurements were made of the exhaust pressure and temperature. The exhaust pressure was measured using a TC sensor (inserted as shown previously in Figure 7). Allowing for area reduction (which is small) the pressure readings for nitrogen flows using a similar development as above gave values within 5% of those estimated by the Poiseville equation. Next, a thermocouple was inserted in the center of the exhaust line. The reading was 89°C for the nitrogen flow simulation. Allowing for heat loss and differences in heat capacities, 100°C was estimated as the gas temperature. This value was used in calculations of flow kinetics and the absorption discussion. It can be considered only as a reasonable estimation since it could not be actually measured in the wafer vicinity.

3.4.4.2.3 CHEMICAL KINETICS

To obtain a deposition model, a review of basic chemical kinetic theory defines three areas of investigation for a chemical reaction: stoichiometry, kinetics, and mechanisms. In general the stoichiometry is studied first, and then the kinetic effects are considered. Finally, a mechanism model is developed. For the silicon nitride deposition process, the chemical equation is normally written as:

$$3\ SiH_2Cl_2(g) + 4\ NH_3(g) \rightarrow Si_3N_4(S) + 6\ H_2\ (g) + HCl(g).$$

For reactions in which conditions have a much greater effect than molar composition, multiple reaction is evidenced. Also, phase changes and molecular complexing provide further indication that the reaction can not be easily analyzed using normal stoichiometric rate methods (26). Often when one component of a binary reaction is in great excess (or regenerated) the reaction rate is controlled by the concentration of the other component. For the gas mixture commonly used, this is the situation for the deposition reaction; however, this is not valid for lower ratios. Since the literature review on other CVD reactions indicated kinetic properties as rate-limiting, analysis of kinetic theory was pursued first.

The general chemical rate equation can be written as the product of a composition-dependent term and a temperature-dependent term (27):

$$r = f_1\ (\text{temperature})\ f_2\ (\text{composition}).$$

Reaction kinetics are based upon the temperature-dependent relation which is represented by Arrhenius' theory where the reaction rate is found as (18):

$$r = k.f_2\ (\text{composition})$$

and $k = A\ e^{-Ea/RT}$

A = pre-exponential factor

E_a = activation energy of reaction, kcal mol^{-1}.

Written in logarithmic form, it becomes

$$\log k = \frac{-Ea}{2.303RT} + \log A.$$

This is a linear equation of the log k versus the reciprocal of temperature. Over moderate temperature intervals, the slope of this equation yields the activation energy which is required for the reaction to proceed. A plot of deposition rate as a function of reaction temperatures is given in Figure 13 as plot (a). The activation energy is 67.2 kcal. (Due to some data scatter from other influencing variables and the small temperature interval, a reasonable error of ± 5% should be expected.) This energy is comparable to the more temperature sensitive reaction using silane and ammonia whose activation energy has been estimated as 52 kcal mol^{-1}. Further, it is also approximately the bond dissociation energy for the Si-Cl bond (18).

3.4.4.2.4 COLLISION THEORY

According to molecular collision theory, the reaction rate is a function of the number of molecule collisions and the fraction that involve sufficient energy to react. So, the second order rate constant should be given by (25):

$$k = \frac{dC/dt}{[A\ B]}$$

A, B, C = reactant concentrations

$$\frac{dC}{dt} = \frac{Z_{12}}{N_A}$$

Z_{12} = number of collisions between unlike molecules, sec^{-1}

N_A = Avogadro's number, mol^{-1}

C = number of reactant molecules per unit volume, cm^{-3}

$$[A]\ [B] = (n_1/N_A)(n_2/N_A) = \frac{n_1 n_2}{N_A^2}$$

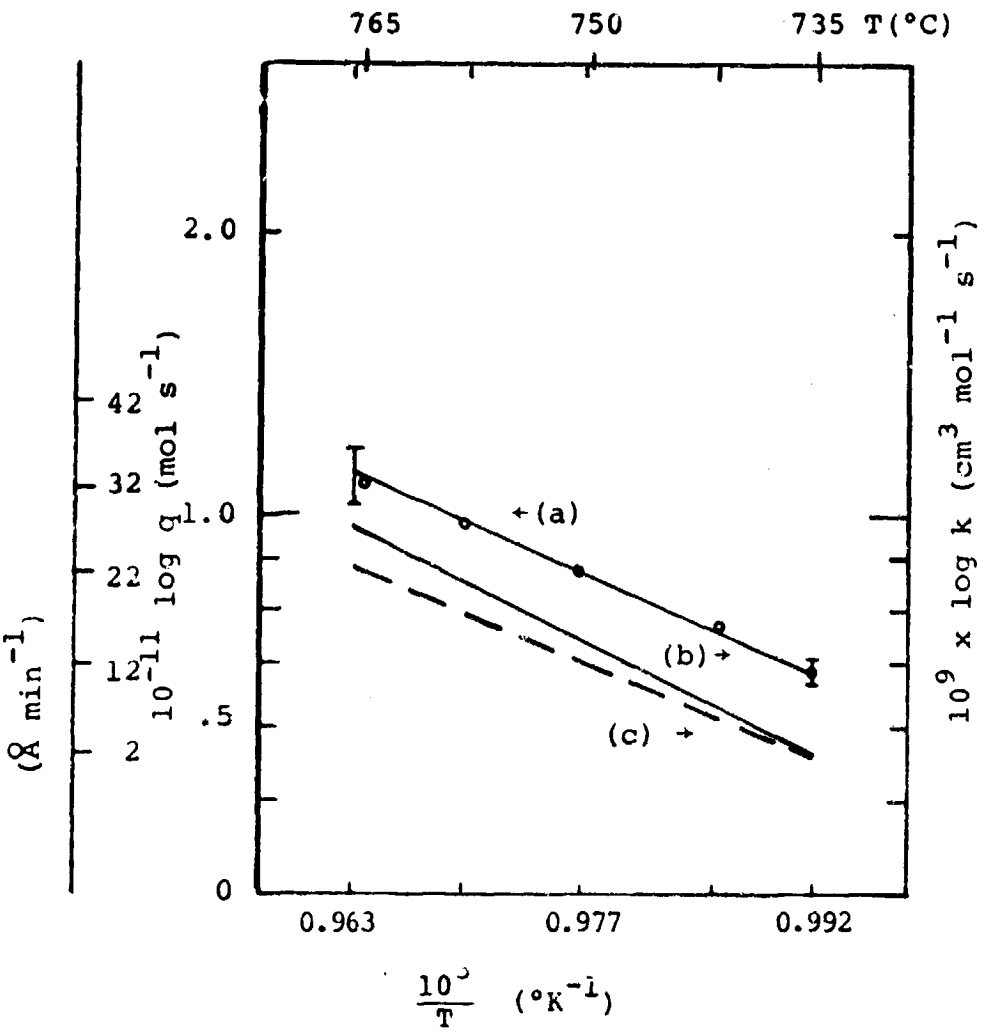


FIGURE 13: ARRHENIUS TEMPERATURE DEPENDENCE PLOT (a) MEASURED DEPOSITION RATE
(b) CALCULATED SECOND-ORDER RATE CONSTANT (150 wafer area)
(c) CALCULATED SECOND-ORDER RATE CONSTANT (75 wafer area)

For a binary gas reaction:

$$k = \frac{N_A Z_{12}}{n_2 n_1} \quad .$$

Including the energy function gives:

$$k = \frac{N_A Z_{12}}{n_1 n_2} \left[p e^{-E_o/RT} \right]$$

where p is the steric fraction which is introduced to allow for the fact that a certain orientation is required for the reaction of polyatomic molecules.

The minimum reaction energy, E_o can be normally related to the Arrhenius activation energy by (25):

$$E_a = E_o + \frac{RT}{2} \quad .$$

Since $$\frac{RT}{2} \approx 1 \text{ kcal/mol}$$

$$E_o \approx 66 \text{ kcal/mol}$$

The rate equation can be written as (26):

$$\text{rate} = P \left[\frac{8\pi RT(M_1+M_2)}{M_1 M_2} \right]^{\frac{1}{2}} \sigma_{12}^2 \, e^{-\Delta E_o/kT} \, [A] \, [B]$$

where P = steric factor (10^{-5}).

Thus the Arrhenius pre-exponential factor is found to be:

$$A = 4.7 \times 10^4 \frac{cm^3}{mol.s}$$

The rate constant is

$$k = A \, e^{-\Delta E_o/KT}$$

$$= 3.7 \times 10^{-5} \text{ cm}^3/\text{mol.s}$$

This value of the rate constant is extremely low and negates the application of free gas biomolecular collision as a reaction mechanism. These calculations assumed a high gas reaction temperature. But at a temperature of 100°C, which

is believed to be the actual gas temperature, the reaction constant becomes on the order of 10^{-30} cm^3/mol.s; thus, no reaction can occur in the free gas stream. To provide another possible rate comparison and to help evaluate the steric factor, transition state reaction theory was investigated.

3.4.4.2.5 TRANSITION STATE THEORY

According to transition-state theory, the reactants form an activated, intermediate complex which decomposes into the observed products (29). The mechanism is illustrated in the following second order reaction:

$$A + B \rightleftarrows [AB]^* \rightarrow \text{products.}$$

reactants — Activated Complex

Since Arrhenius theory is a specific extension of this theory, the activation energy found by the Arrhenius plot is the amount of energy required to form the complex and is graphically represented in Figure 14. Since the activated complex is not merely an intermediate compound but a mechanism of breaking or forming bonds, the rate of reaction can be determined as changing a vibration mode to a translation given by quantum theory (28). The rate is expressed as (18):

$$k = \left(\frac{kT}{h}\right) \omega \left(\frac{Q^*}{Q_A Q_B}\right) C_A C_B \; e^{-E_o^*/RT}$$

where ω = transmission coefficient (≈ 1)

Q = Partition function

$Q_i = q_{trans}\, q_{rot}\, q_{vib}$

For reactions including no nonlinear reactant molecules, such as dichlorosilane and ammonia, the pre-exponential factor is generally on the order of 10^4 cm^3 $mol^{-1}s^{-1}$ assuming a steric factor of 10^{-5}. The steric factor is found as (29):

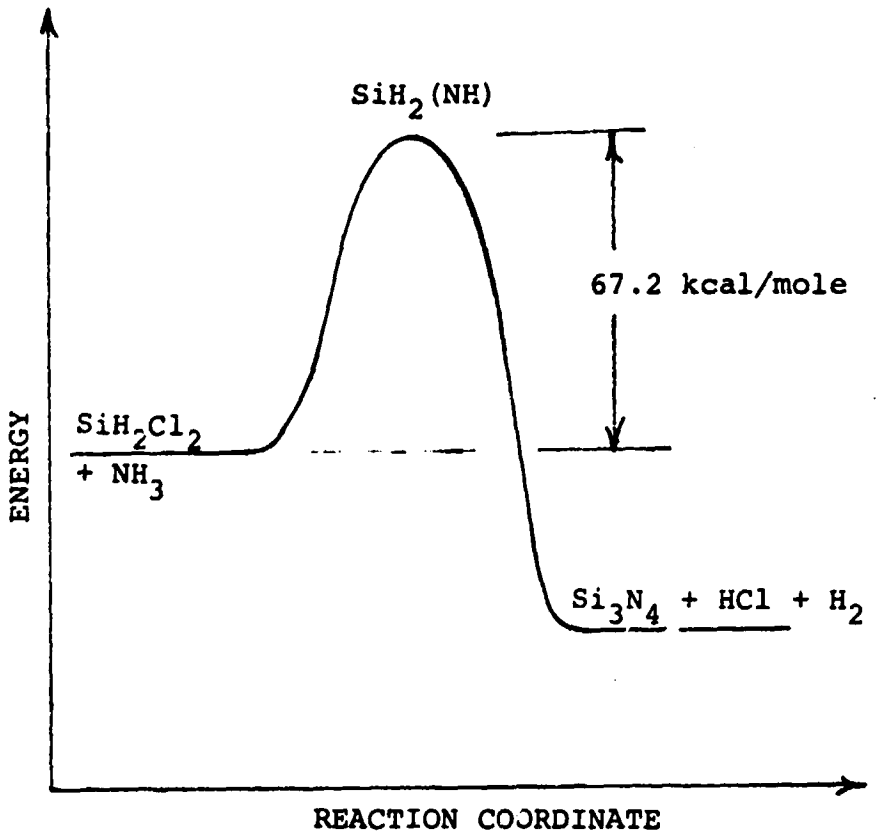


FIGURE 14: SIMPLIFIED REACTION COORDINATE DIAGRAM SHOWING THE AMINOSILANE COMPLEX AS THE TRANSITION STATE WITH THE ACTIVATION ENERGY BARRIER.

$$P = \left(\frac{qv}{qr}\right)^5$$

The reaction rate would be similar to that predicted by collision theory, and many orders of magnitude too small. This does not appear to be consistent with the fact that the formation of intermediate complexes such as silicam and other aminosilanes have been shown. To evaluate this mechanism further, a second order reaction is considered.

3.4.4.2.6 SECOND ORDER REACTION

As previously noted, an intermediate reaction has been discussed as a possible rate-determining mechanism for the overall reaction. One such reaction is given in reference 29 by Stock and Someski who studied the following dichlorosilane and ammonia reaction:

$$SiH_2Cl_2 + NH_3 \xrightarrow{k} SiH_2(NH) + 2\,HCl \quad .$$

The resulting monoiminosilane polymerizes immediately, and above 600°C decomposes quickly to α-silicon nitride. Assuming that breaking the Si-Cl and N-H bonds, both of which require approximately 60 - 65 kcal/mole, would be slower than the polymerization, then the decomposition of the unstable aminosilane complexes would be the controlling chemical reaction. Thus, a second order reaction rate equation for the above reaction can be expressed as:

$$\frac{d[SiH_2(NH)]}{dt} = k\,[SiH_2Cl_2][NH_3]$$

where the brackets [ ] represent molar concentration of the reactants. The integrated form is given by:

$$k = 2.303 \log \frac{\left[SiH_2Cl_2\right]_i \left[NH_3\right]_f}{\left[SiH_2Cl_2\right]_f \left[NH_3\right]_i} \Big/ t\,(\left[NH_3\right]_i - \left[SiH_2Cl_2\right]_i)$$

where $[SiH_2Cl_2]_i \neq [NH_3]_i$.

The initial (i) and final (f) concentrations of the reactants after the time interval (t) are calculated as follows:

1. $[SiH_2Cl_2]_i = \frac{\mathring{n}_1}{\Sigma \mathring{n}_i} \frac{P}{RT} = \frac{p_1 mm}{RT}$,

where $\mathring{n}_i$ = inlet meter rate, $\Sigma \mathring{n}_i$ = total flow rate, P = system pressure, and $p_1 mm$ = partial pressure.

2. $[NH_4]_i = \frac{\mathring{n}_2}{\Sigma \mathring{n}_i} \frac{P}{RT} = \frac{p_2 mm}{RT}$

3. $[SiH_2Cl_2]_f = \frac{(\mathring{n}_1 - 3q)}{\Sigma n_i} \frac{P}{RT}$

where q is the deposition rate of Si_3N_4. (The rate of consumption of dichlorosilane by the chemical reaction is three time q.)

The values used in the analysis were:

$R = 6.232 \times 10^4$ mm cm^3 $^oK^{-1}$ s^{-1}

$P = 0.5$ mm

$\mathring{n}_1 = 8.086 \times 10^{-6}$ mol s^{-1}

$\mathring{n}_2 = 2.286 \times 10^{-5}$ mol s^{-1}

$\Sigma n_i = 3.095 \times 10^{-5}$ mol s^{-1}

$T_g = 100^oC$

$T_s = 725^oC$. (wall temperature)

Also, the gas residence time was assumed to be 20 sec. from flow kinetics values. Since the concentration of NH_3 is much greater than that of dichlorosilane, the initial and final values for ammonia were considered equal, i.e. $[NH_3]_i \simeq [NH_3]_f$. Substituting this assumption and the above data, the rate equation now relates the rate constant (k) to the reaction temperature (T_s) and the silicon nitride deposition rate (q) as follows:

$$k = 9.02 \times 10^{6} T_S \log \left[\frac{\dot{n}_i}{\dot{n}_1 - 3q} \right] \text{ cm}^3 \text{ mol}^{-1} \text{ s}^{-1}.$$

The Arrehenius plot of the calculated values of k is shown in Figure 13 as plot (b). In general the slope is approximately the same as the deposition rate plot but begins to change at higher temperatures. The activation energy is 65.9 kcal mol^{-1}. This variation is explained since the reaction area for 150 3 inch wafers was used in the calculations. The constant concentration of ammonia no longer is valid, and reaction depletion affects the calculated values. This is observed in actual operation and is compensated for by a temperature increase or use of fewer wafers. To verify this behavior, a reduced deposition area (75 3 inch wafers) was used in the calculation, resulting in curve (c), Figure 13, which has the same slope as the deposition rate plot.

To compare the deposition rate predicted by using the second order rate constant the following calculation was performed:

$$\text{rate} = k \, [SiH_2Cl_2]_i \, [NH_3]_i$$

where $k = 5.434 \times 10^{9} \text{ cm}^3 \text{ mol}^{-1} \text{ s}^{-1}$

at $T = 750^{\circ}C$

$[SiH_2Cl_2]_i = 6.987 \times 10^{-9} \text{ mol cm}^{-3}$

$[NH_3]_i = 1.975 \times 10^{-8} \text{ mol cm}^{-3}$

so $\text{rate} = 7.546 \times 10^{-7} \text{ mol cm}^{-3} \text{ s}^{-1}$

Assuming the deposition is on 75 3 inch wafers, this would give a deposition rate of 9.432×10^{-1} mol cm^{-2} s^{-1} or 23Å min^{-1}. This compares to a 22Å min^{-1} measured rate (which includes some error associated with estimating reactor deposition area).

3.4.4.2.7 SURFACE COLLISION RATE

Since the collision theory for molecule-to-molecule collisions did not agree with observations, absorption based on molecules striking a surface was

investigated for a kinetic relationship. As shown before, the collision rate with a surface is given by:

$$\nu = 3.513 \times 10^{22} \frac{Pmm}{(MT)} 1/2 \ cm^{-2} \ s^{-1} \quad .$$

For dichlorosilane at T = 100°C,

$$\nu = 2.369 \times 10^{19} \ cm^{-2} \ s^{-1} \quad .$$

Since there are 3 dichlorosilane molecules for a deposited molecule of silicon nitride, then the deposition rate is:

$$g = 7.107 \times 10^{18} \text{ molecules } cm^{-2} \ s^{-1} \quad .$$

For a reaction for two nonlinear molecules such as ammonia and dichlorosilane, the steric factor, or reaction probability, is normally given as 10^{-5} (28). At similar temperature and atomic mass (20, 31), dichlorosilane molecules will have a gas striking coefficient of 0.6 to 0.7. (The striking coefficient is the percentage of collisions that results in surface absorption.) Assuming the above factors, the projected deposition rate will become approximately:

$$g = 4.5 \times 10^{13} \text{ molecules } cm^{-2} \ s^{-1} \quad .$$

For an actual deposition of 22Å min^{-1} of silicon nitride, the rate can be written as:

$$g = 5.413 \times 10^{13} \text{ molecules } cm^{-2} \ s^{-1} \quad .$$

This is very close to the predicted rate above based on absorption surface collisions of dichlorosilane molecules and a second order reaction with ammonia.

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3.5 ION IMPLANTATION TECHNOLOGY

The objective of this study is to perform a detailed systematic investigation of solar cell characteristics influenced by implant conditions (voltage, beam current, beam traversals, dose), impurity species (P, As, B), cell type (n-on-p, p-on-n), and anneal cycle.

3.5.1 ION IMPLANTER CALIBRATION

A series of calibration ion implantations was performed on the high beam current implanter. Implants were made with boron (B^{11}), phosphorous (P^{31}), and Arsenic (As^{75}). These tests were conducted with polished <100> silicon wafers, the necessary substrate orientation if effective texture etching is to be considered. For boron implants, n-type test wafers with resistivities between 5 and 7 Ω-cm were used. For phosphorous and arsenic implants, p-type test wafers with resistivities between 0.6 and 1.4 Ω-cm were used. Boron and phosphorous implants have been performed at implant angles of 5.5 and 7 degrees, not a significant difference, while arsenic implants have been performed only at 7 degrees.

The two major parameters which determine the properties of an implanted layer are ion acceleration energy, expressed in KeV, and ion dose, expressed in ions per cm^2. Implants have been performed at energies ranging from 35 KeV to 195 KeV, essentially the limits of the implanter being used. Ion doses studied ranged between 10^{14} cm^{-2} and 10^{16} cm^{-2}. The range between these two doses encompasses all implants of interest for silicon solar cells.

One primary selling point for the implanter being used is its capability of high ion beam currents (a minimum of 2 mA for P^{31} or As^{75} and 1 mA for B^{11}). High beam current means that less time is required to achieve a specified dose.

Unfortunately, mechanical limitations in transporting wafers negate this advantage to some extent when lower doses are desired. Figure 15 shows the correlation between desired dose and required beam current when the implanter is operated in such a manner as to ensure uniformity of the implant across the solar cell surface, using the manufacturer's recommended minimum number of wafer traversals per implant as the criterion. It can be seen that maximum beam current is used only for doses on the order of 2×10^{15} cm^{-2} or greater.

After ion implantation of a silicon wafer surface, an anneal cycle is required to electrically activate the implanted dopants. For calibration purposes, a thermal activation anneal was used whereby test wafers were heated at 900°C for 30 minutes in an atmosphere of nitrogen containing 2% oxygen. The oxygen content is believed to substantially minimize (or eliminate) the occurrence of nitrogen damage to the bare silicon wafers. (In work reported in later sections, other anneal cycles will be compared against this one.) Thirty minutes at 900°C is usually considered sufficient to activate most of the implanted dopant, provided, of course, that the implanted concentration has not exceeded solid solubility at the temperature of anneal.

Sheet resistance data are given as a function of dose in Figures 16, 17, and 18 for boron, phosphorous, and arsenic, respectively. Each of the data points indicated is the mean of sheet resistance measurements at five different points across the surface of each of four different test wafers. Typical standard deviations are in the one to two percent range. These sheet resistance data behave exactly as expected and agree with existing data in the literature, such as those of Bower[1]. Beam current for each total dose, Figures 16, 17, and 18, is the value indicated in Figure 15.

(1) R.W. Bower, Chap. 6, "Device Considerations and Applications," Ion Implantation in Semiconductors, Academic Press, New York, 1970.

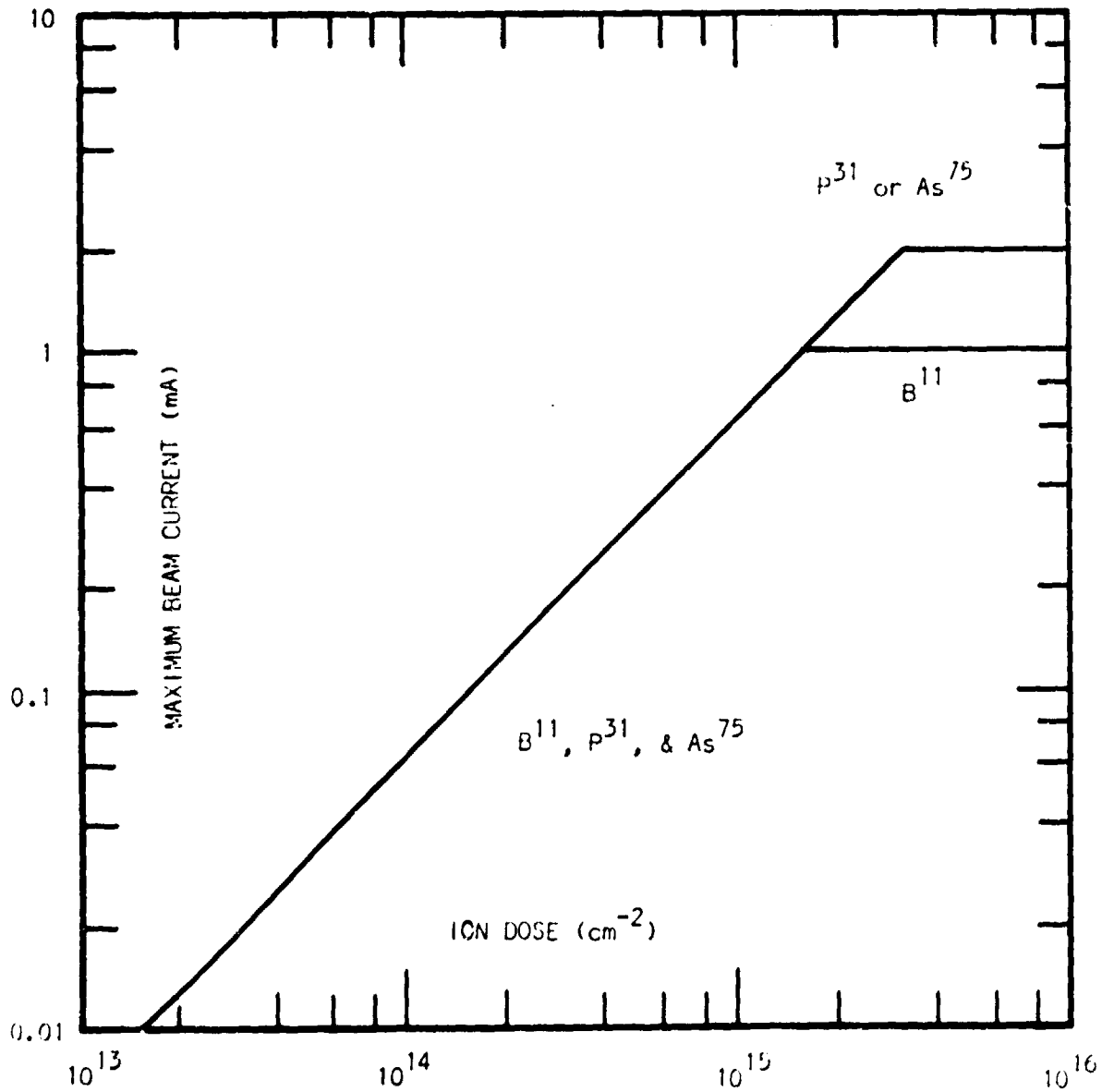


FIGURE 15: MAXIMUM BEAM CURRENT VS DOSE FOR EXTRION 200-1000 ION IMPLANTER, 5 TRAVERSALS PER IMPLANT.

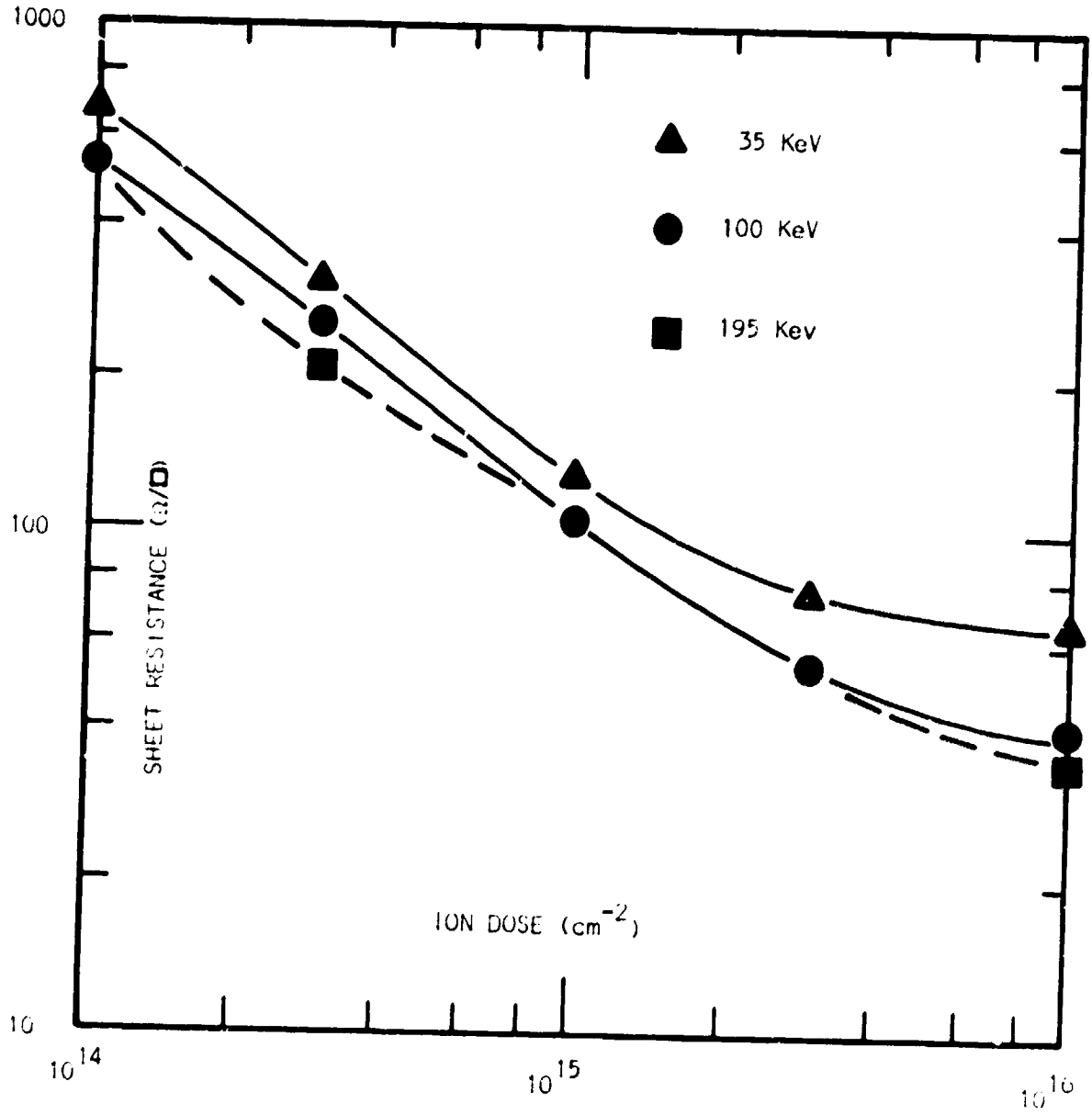


FIGURE 16: JUNCTION SHEET RESISTANCE VS. DOSE AND ENERGY FOR BORON IMPLANT PERFORMED AS DESCRIBED IN THE TEXT.

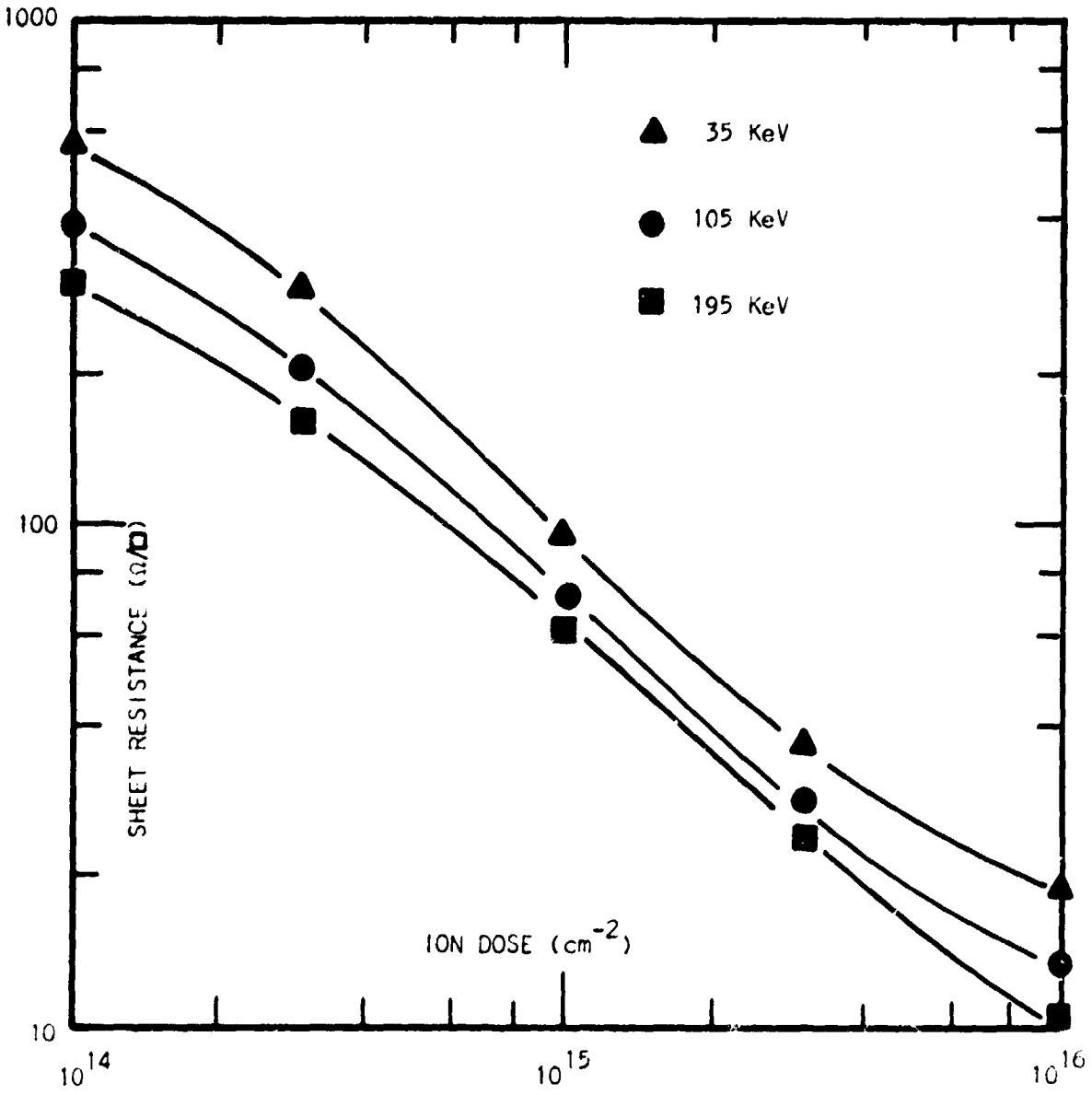


FIGURE 17: JUNCTION SHEET RESISTANCE VS. DOSE AND ENERGY FOR PHOSPHOROUS IMPLANT AS DESCRIBED IN THE TEXT.

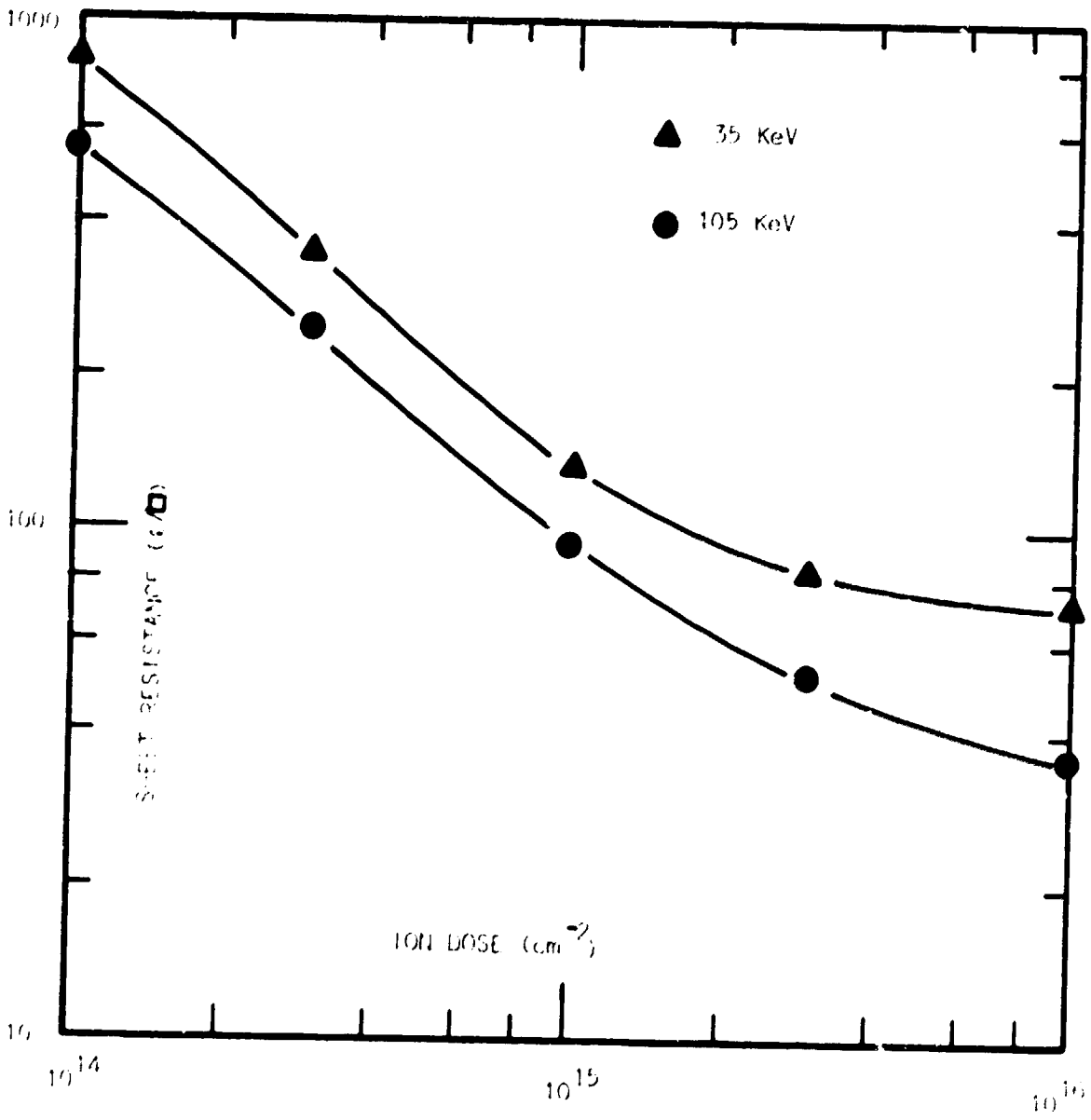


FIGURE 16: JUNCTION SHEET RESISTANCE VS. DOSE AND ENERGY FOR ARSENIC IMPLANT PERFORMED AS DESCRIBED IN THE TEXT.

Listed in Tables 3, 4, and 5 are junction depth data for boron, phosphorous, and arsenic implants, respectively. For any given ion acceleration energy, the penetration depth into silicon will be greatest for boron and least for arsenic. This behavior is exhibited by the data in these tables for the 100 to 105 KeV implants. In this example, the boron junction depth is about 0.9 micron, the phosphorous junction depth is about 0.7 micron, and the arsenic junction depth is about 0.3 micron.

Of course, the junction depth depends on more than implant energy. In particular, the activation anneal cycle can redistribute the implanted impurities through solid state diffusion. The rate of diffusion depends on impurity concentration (dose), anneal temperature, and time. In addition, large differences in dose will cause the Gaussian implanted impurity profile to differ slightly. As exhibited in Table 4, the phosphorous junction depth tended to be greater as dose was increased. Other effects peculiar to ion implantation, such as ion channeling, will also influence the actual junction depth.

3.5.2 PHOTORESPONSE AS A FUNCTION OF IMPLANT ENERGY AND DOSE

Experiments have been performed with phosphorous (P^{31}), boron (B^{11}), and arsenic (As^{75}) implants into bare, smooth wafers. Implant energies have ranged from 35 KeV to 195 KeV and ion doses have been varied from 10^{14} cm^{-2} to 3×10^{16} cm^{-2} at beam currents up to 2 mA for phosphorous and arsenic and up to 1 mA for boron. In order to make direct comparisons between these different implants, activation anneals have again all been performed utilizing a 30 minute cycle at 900°C.

TABLE 3 : BORON ION IMPLANT JUNCTION DEPTHS

DOSE (cm^{-2})	IMPLANT ENERGY			
	35 KeV	100 KeV	105 KeV	195 KeV
1×10^{14}	0.46 μ	0.76 μ	0.86 μ	--
3×10^{14}	0.52	0.77	0.88	1.08 μ
1×10^{15}	0.49	0.82	0.86	1.08
3×10^{15}	0.48	0.85	0.93	1.11
1×10^{16}	0.52	0.79	0.94	1.14
3×10^{16}	--	--	0.95	1.18

Mean Junction Depth	0.51 μ	0.86 μ	1.12 μ

TABLE 4: PHOSPHOROUS ION IMPLANT JUNCTION DEPTHS

DOSE (cm^{-2})	IMPLANT ENERGY	
	105 KeV	195 KeV
1×10^{14}	--	0.95 μ
3×10^{14}	0.59 μ	0.87
1×10^{15}	0.61	0.91
3×10^{15}	0.67	1.16
1×10^{16}	0.76	1.18
3×10^{16}	--	1.13
Mean Junction Depths	0.66 μ	1.03 μ

TABLE 5: ARSENIC ION IMPLANT JUNCTION DEPTHS

DOSE (cm^{-2})	IMPLANT ENERGY 105 KeV
1×10^{14}	0.22 μ
3×10^{14}	0.26
1×10^{15}	0.24
3×10^{15}	0.26
1×10^{16}	0.44
3×10^{16}	0.35
Mean Junction Depth	0.29 μ

Effects of ion implant parameters on solar cell photoresponse are being studied experimentally. Photoresponse behavior of test solar cells can be observed in Figures 19 through 28. These figures present photogeneration current and open circuit voltage data as functions of ion dose and implant energy. Figures 19 through 23 give data for P^{31} implants, Figures 24 through 26 give data for B^{11} implants, and Figures 27 and 28 give data for As^{75} implants. Arsenic and phosphorous implants were performed into bare, polished, boron-doped, 3 inch diameter test wafers with substrate resistivities between 0.6 and 1.4 Ω-cm. Boron implants were performed into bare, polished, phosphorous doped, 3 inch diameter test wafers with substrate resistivities between 5 and 7 Ω-cm. Subsequent to the implants, the cells were annealed at 900°C for 30 minutes in an atmosphere of nitrogen with 2% oxygen. The small percentage of oxygen was used in the nitrogen ambient to prevent the possibility of nitrogen damage to the silicon surface.

After the anneal, the bare test cells were electrically characterized. Open circuit voltage was measured under a quartz-halogen lamp at one sun intensity by using a high impedance digital voltmeter (Keithley). Under the same lamp, photogeneration current was measured by observing the reverse biased diode characteristics with a curve-tracer (Tektronix). The generation current behavior can be observed in the third quadrant, even though, with no metal contacts yet applied, the cell has appreciable internal resistance. The current and voltage thus measured are indicative of solar cell performance.

Several conclusions can be drawn from the data of Figures 19 - 28. First, overall performance of the test solar cells is very reasonable, considering that no antireflective coating or texture etching was used. Of course, larger current and voltage values will be obtained when an anti-

FIGURE 19

PHOTORESPONSE DATA: 35 KeV PHOSPHOROUS

IMPLANT AT 7 DEGREE ANGLE

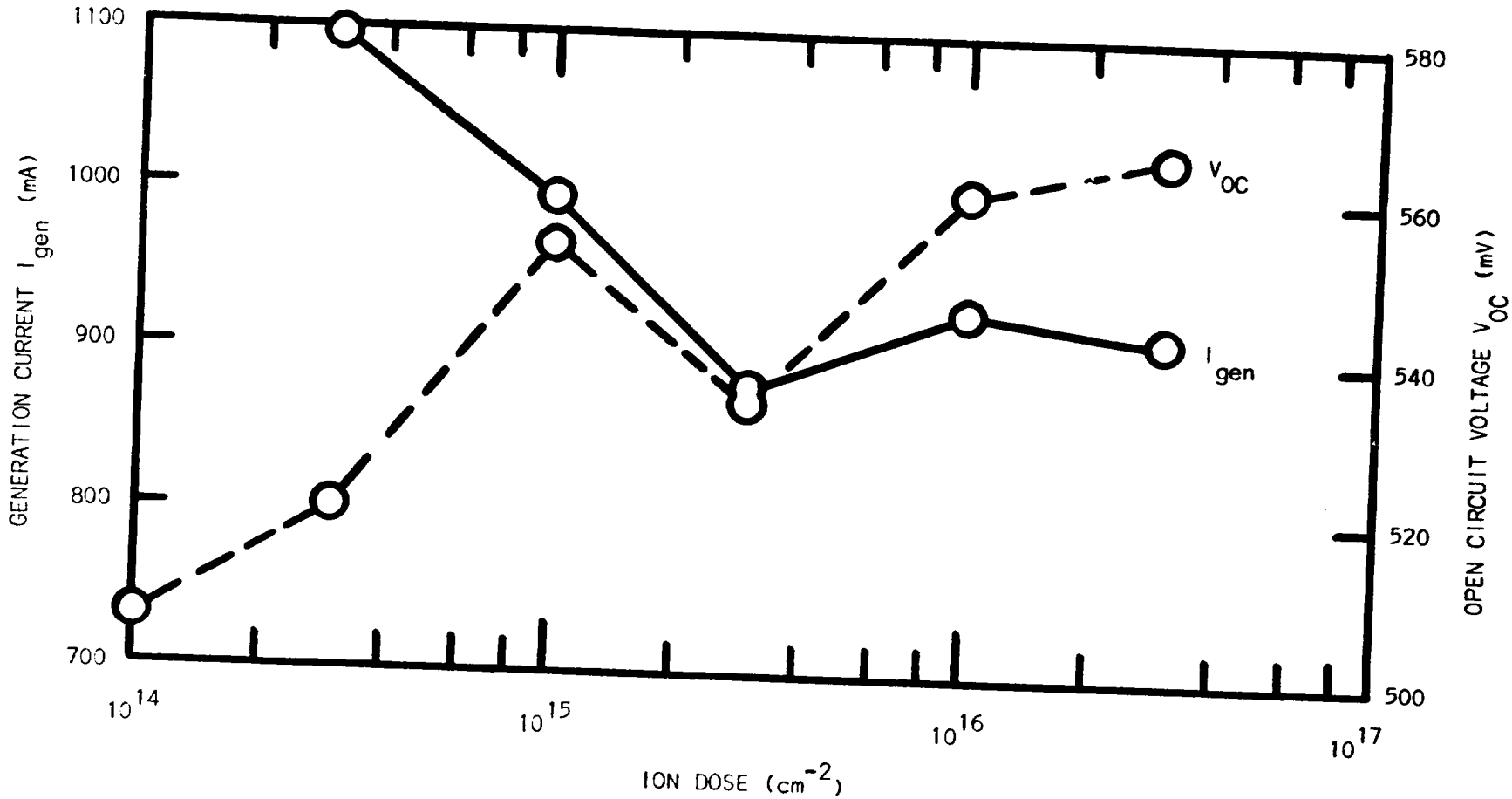


FIGURE 20

PHOTORESPONSE DATA: 105 KeV PHOSPHOROUS

IMPLANT AT 7 DEGREE ANGLE

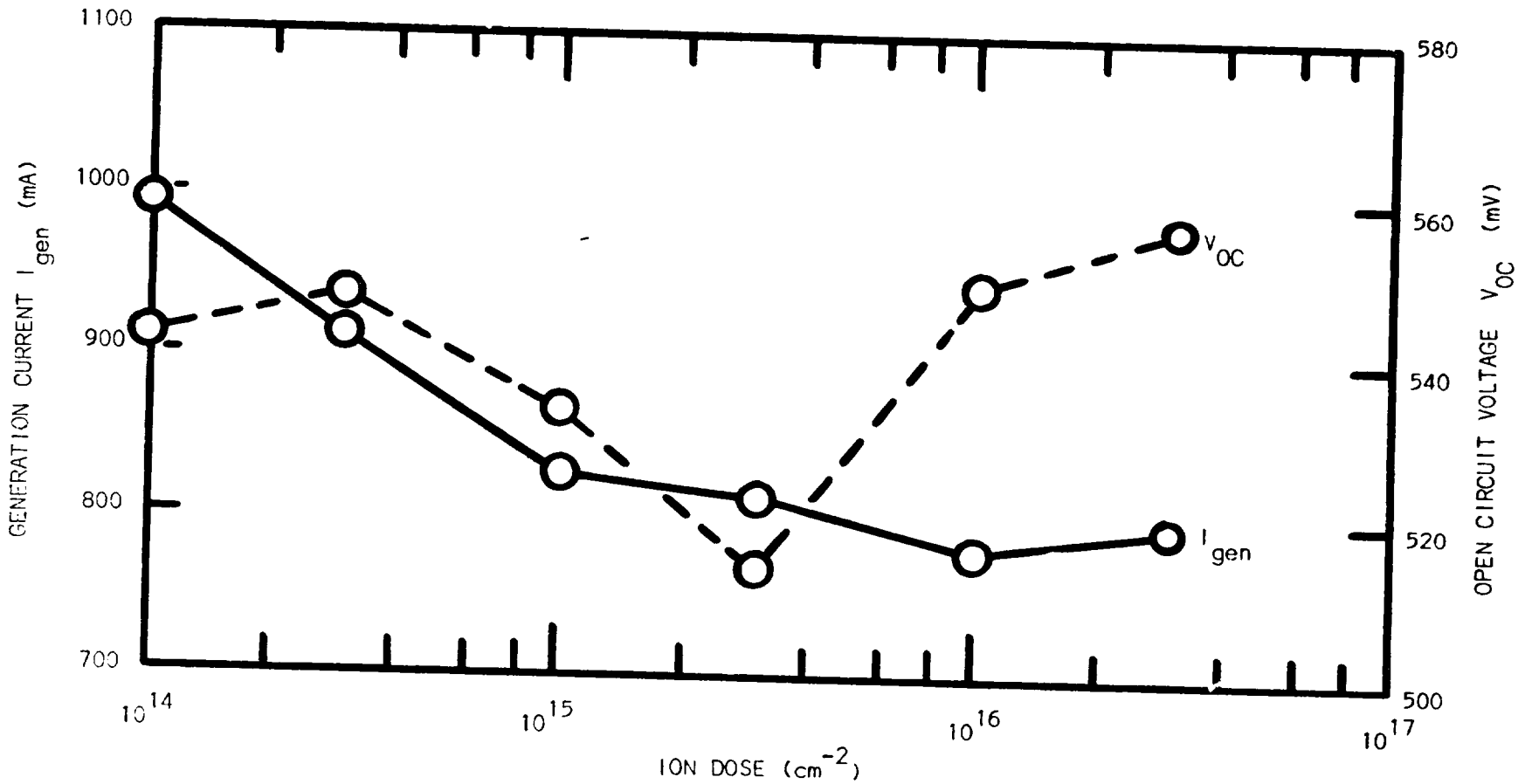


FIGURE 21

PHOTORESPONSE DATA: 105 KeV PHOSPHOROUS

IMPLANT AT 5.5 DEGREE ANGLE

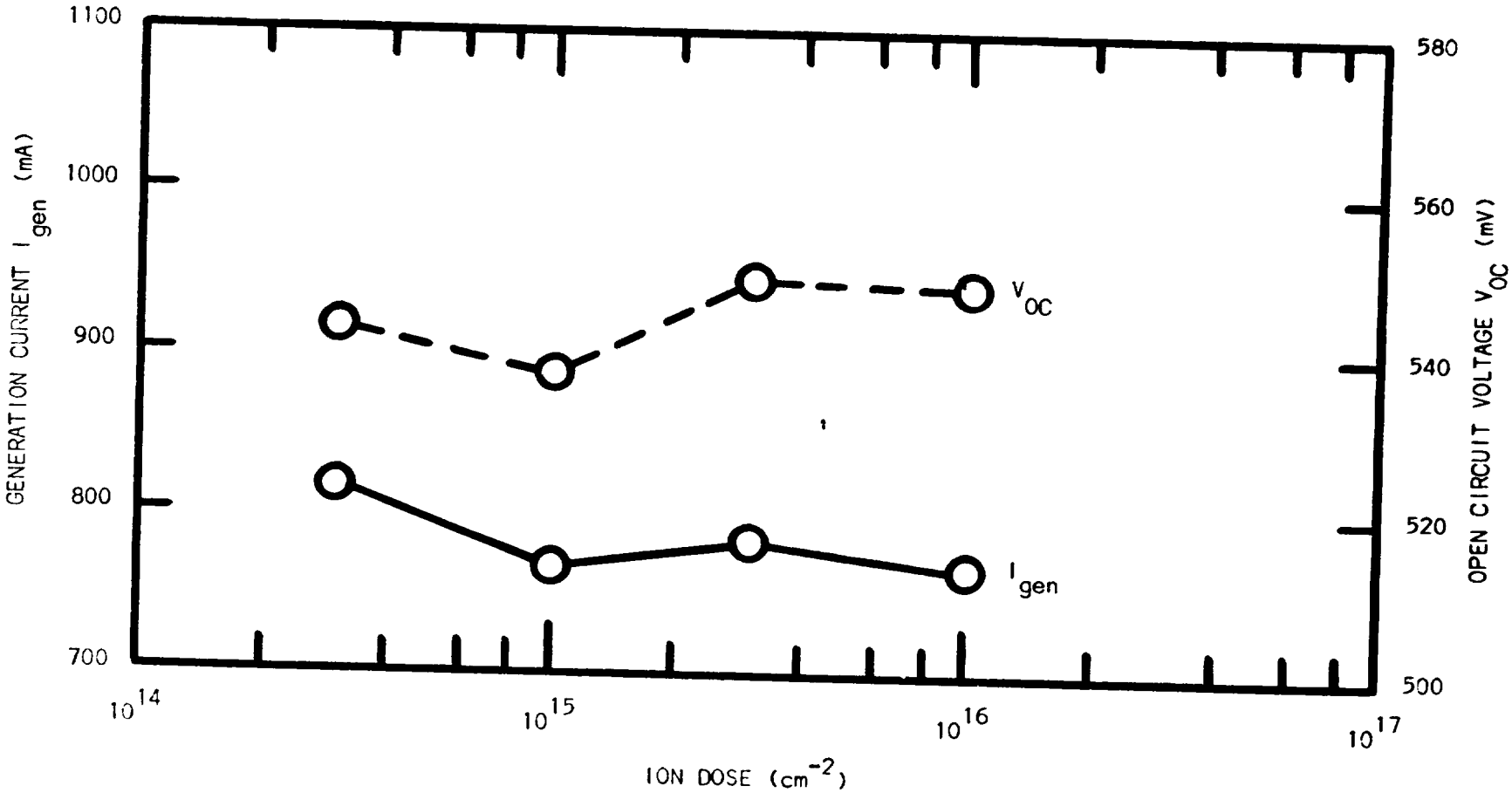


FIGURE 22

PHOTORESPONSE DATA: 175 KeV PHOSPHOROUS

IMPLANT AT 5.5 DEGREE ANGLE

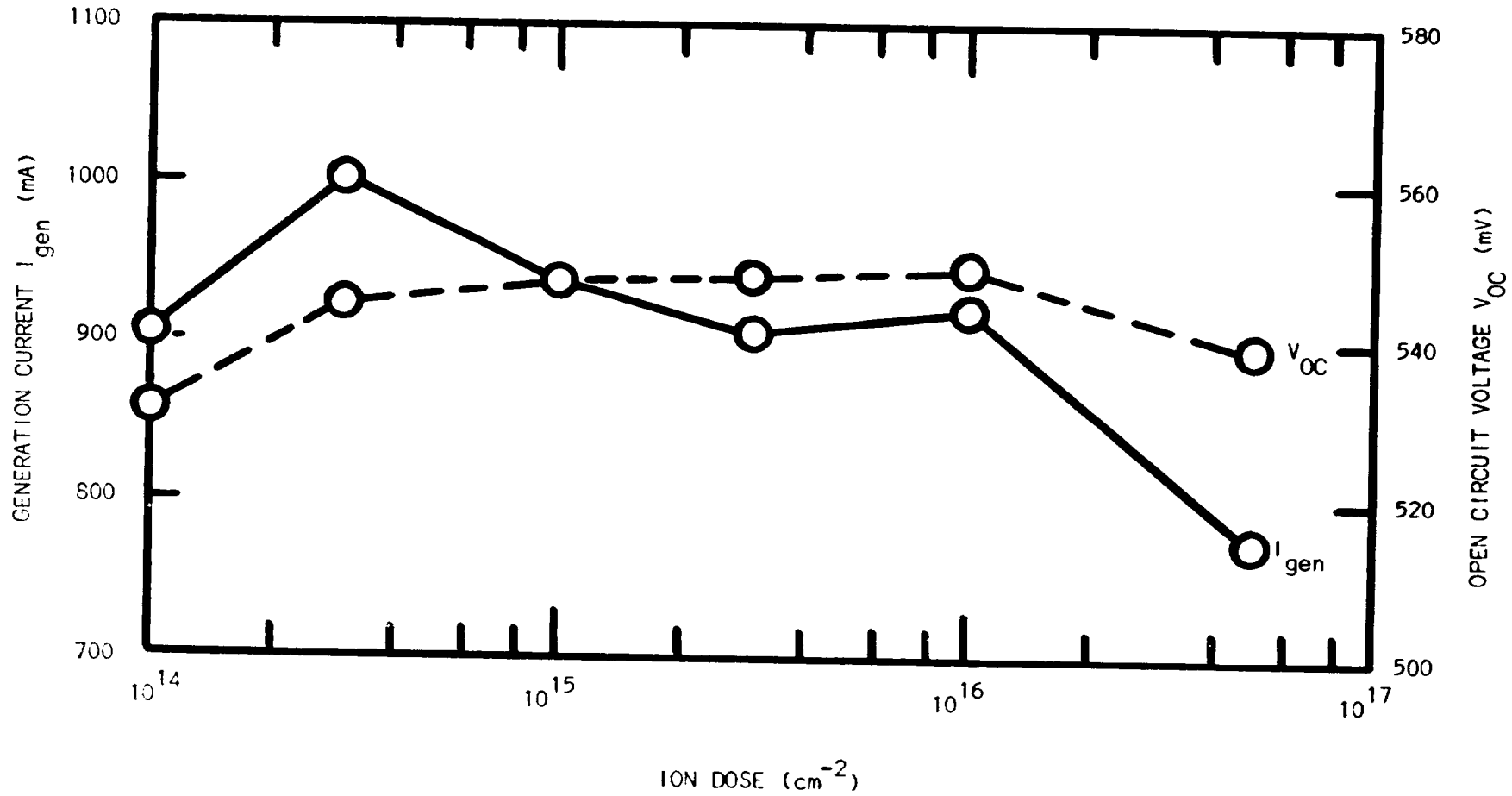


FIGURE 23

PHOTORESPONSE DATA: 195 KeV PHOSPHOROUS

IMPLANT AT 5.5 DEGREE ANGLE

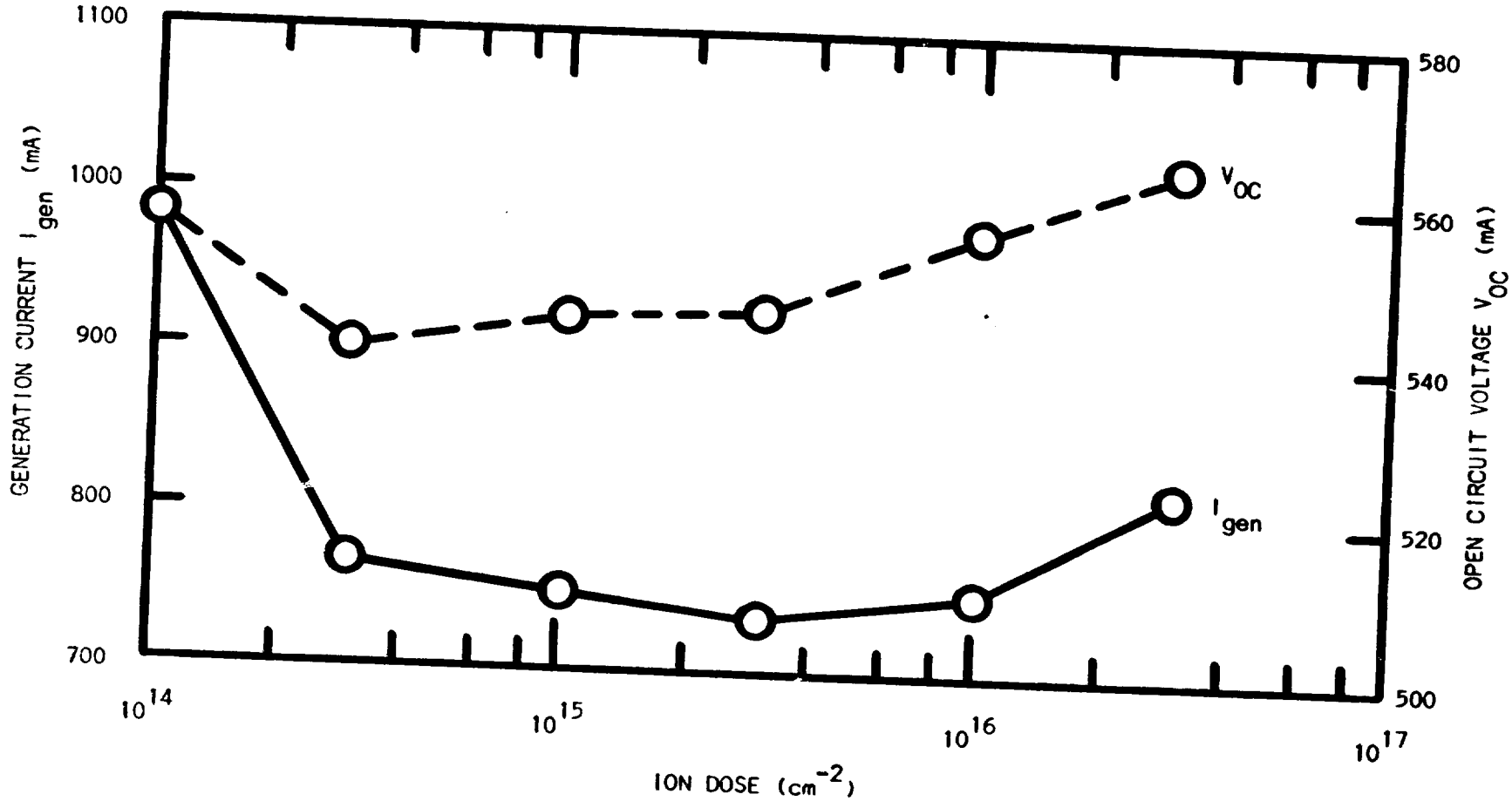


FIGURE 24

PHOTORESPONSE DATA: 35 KeV BORON

IMPLANT AT 5.5 DEGREE ANGLE

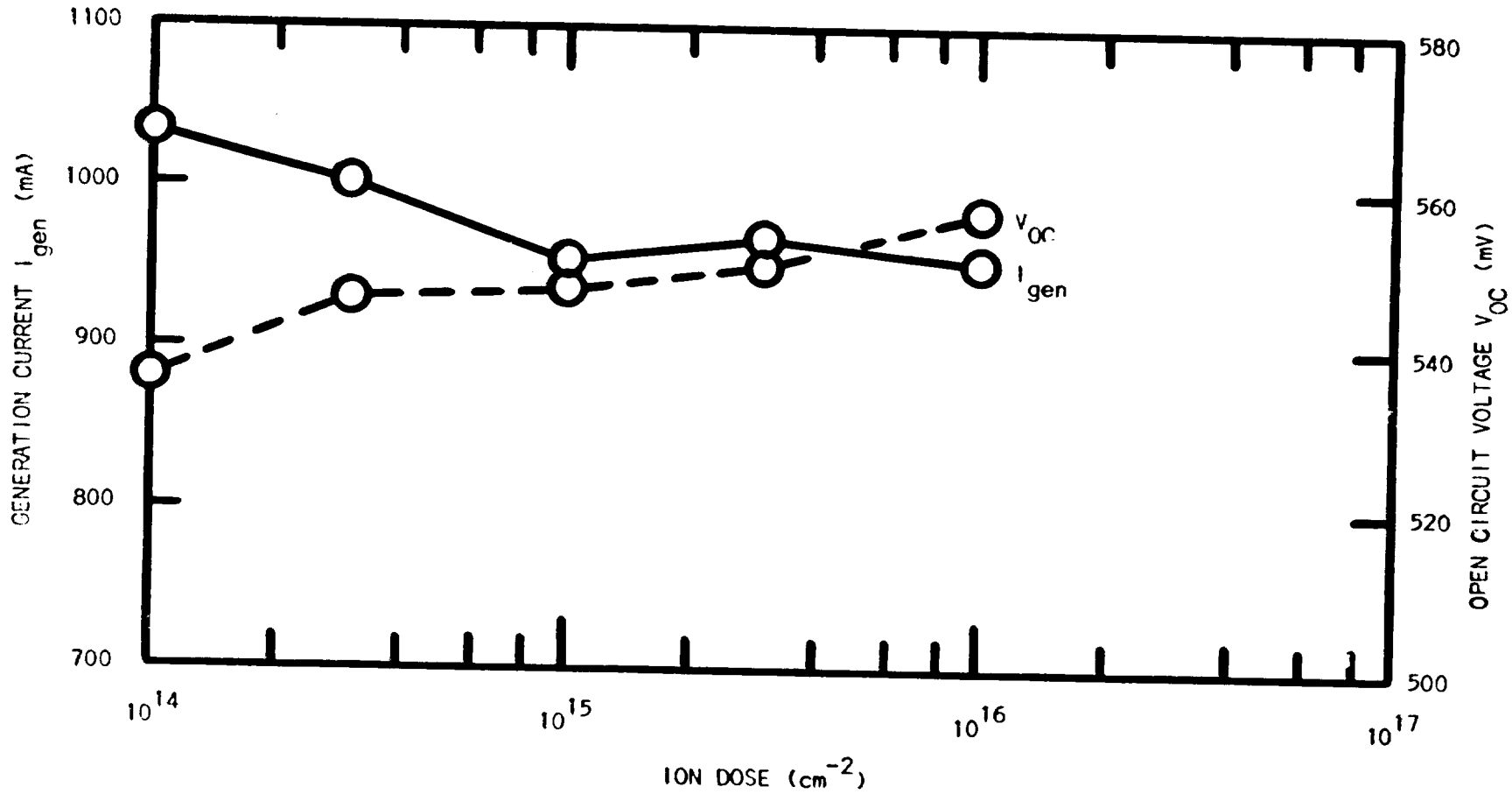


FIGURE 25

PHOTORESPONSE DATA: 100 KeV BORON

IMPLANT AT 5.5 DEGREE ANGLE

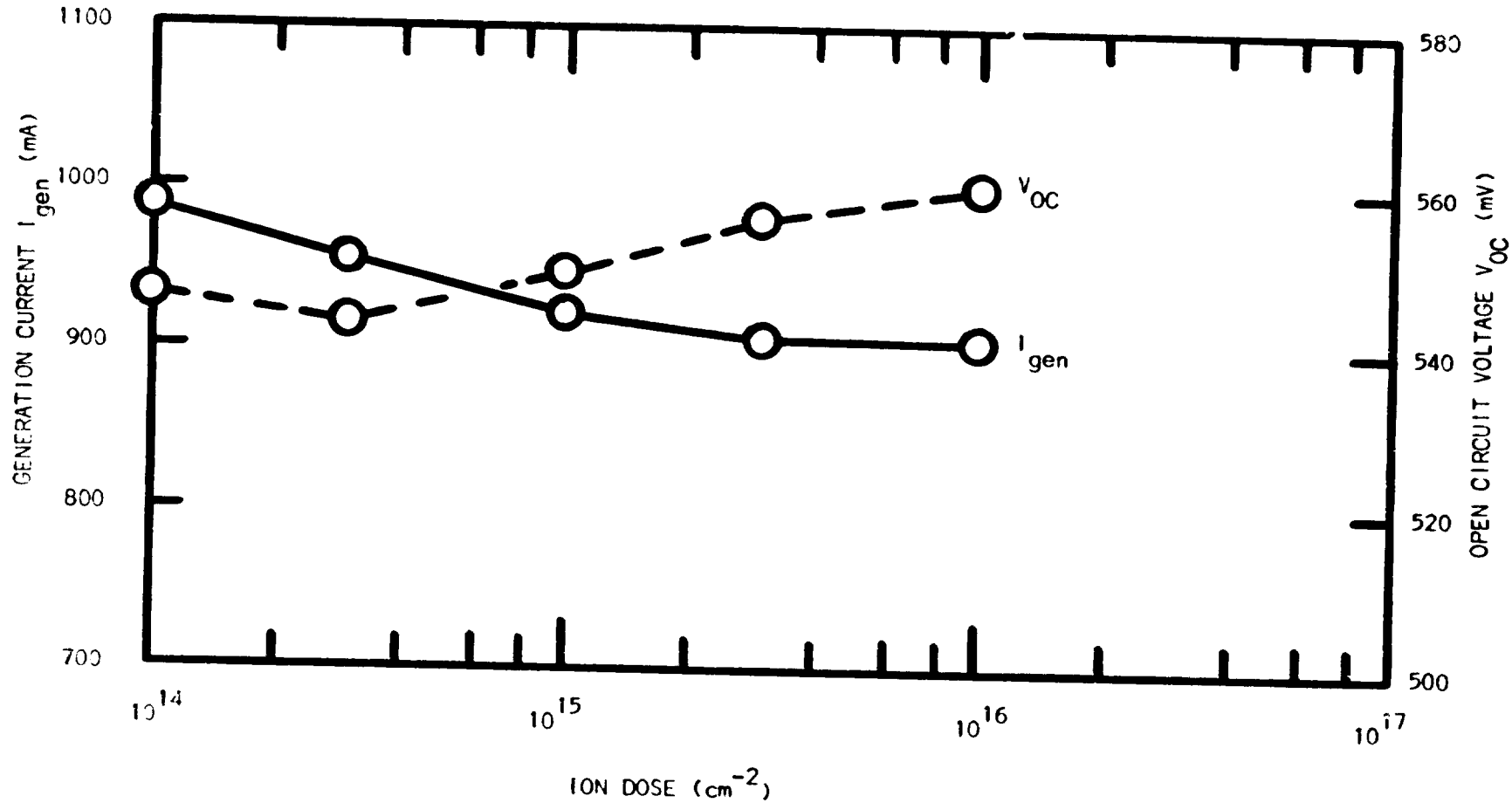


FIGURE 26

PHOTORESPONSE DATA: 195 KeV BORON

IMPLANT AT 5.5 DEGREE ANGLE

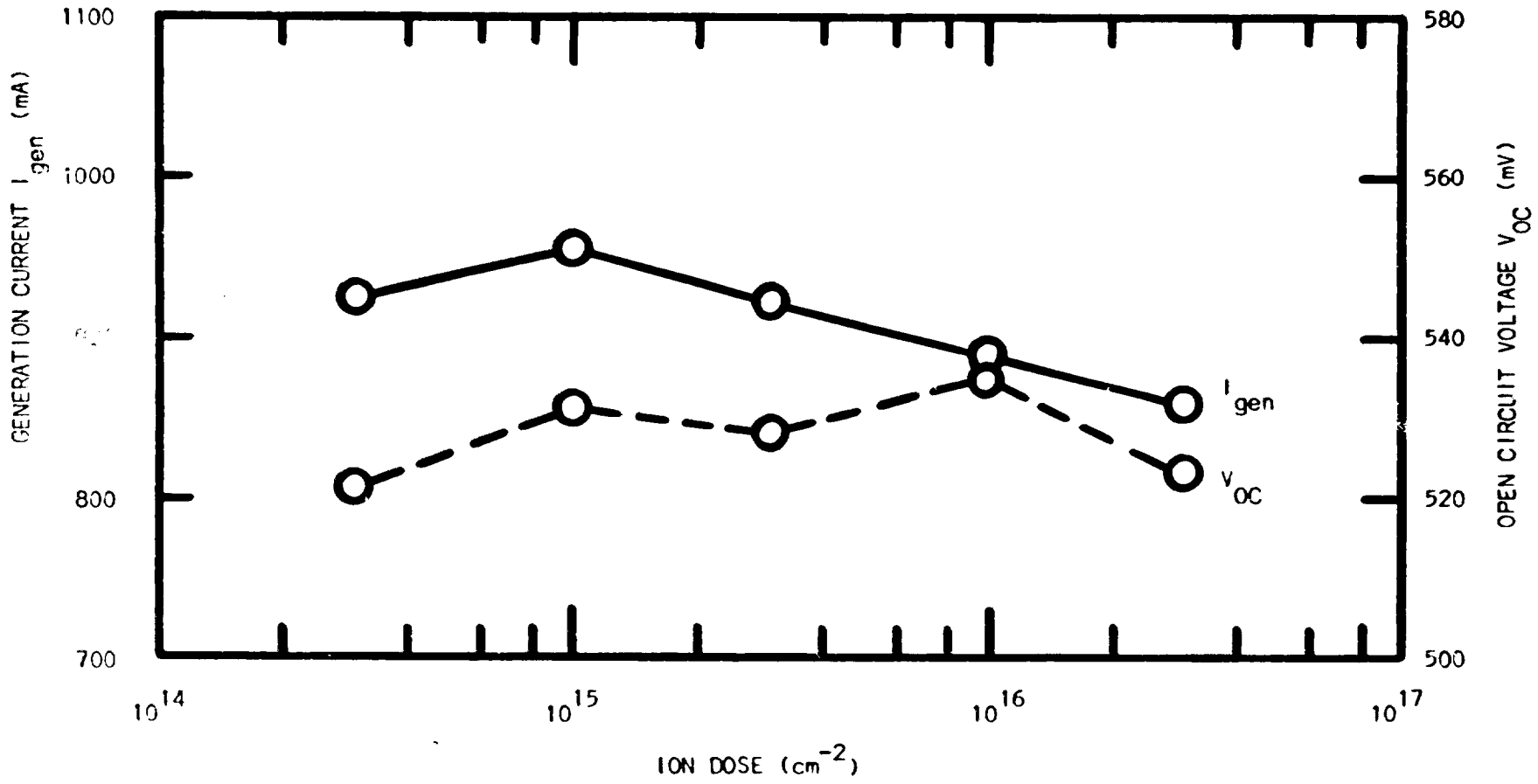


FIGURE 27

PHOTORESPONSE DATA: 105 KeV ARSENIC

IMPLANT AT 7 DEGREE ANGLE

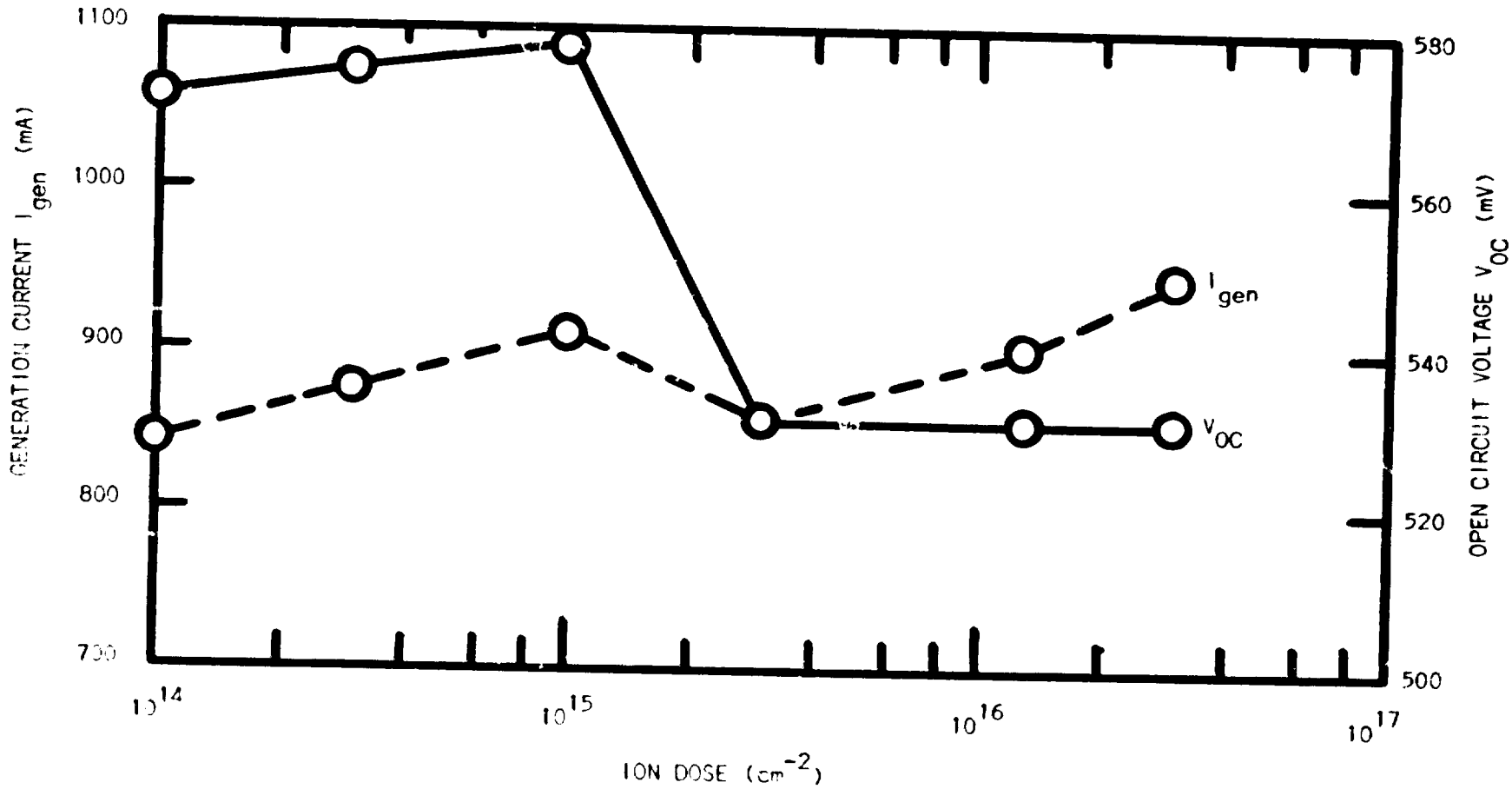
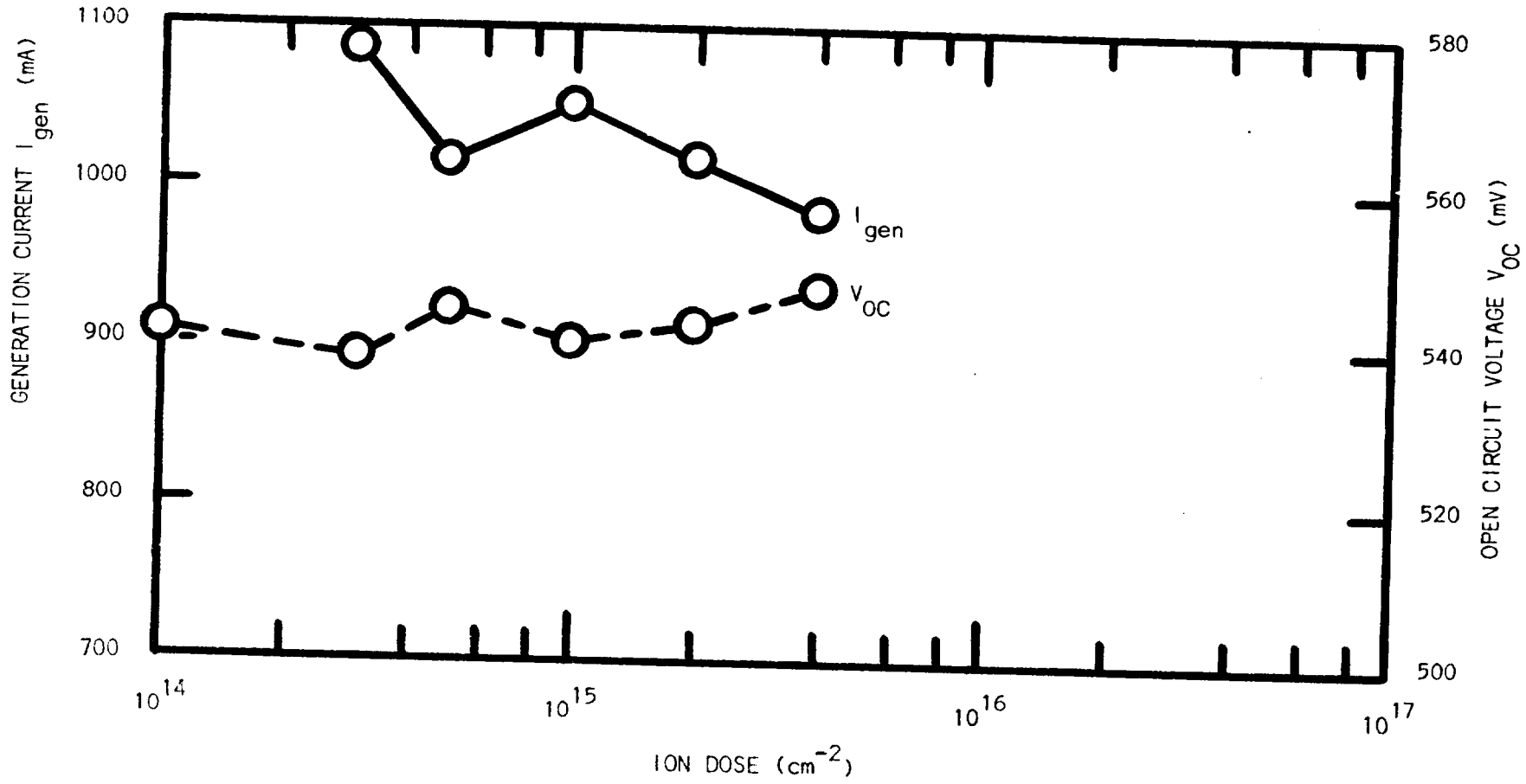


FIGURE 28

PHOTORESPONSE DATA: 195 KeV ARSENIC

IMPLANT AT 7 DEGREE ANGLE



reflection coating and metal contacts are applied. (Photocurrent should be about 50% higher, and V_{OC} should be increased by about 35 mV; if this proves to be the case in completed cells, then both n-on-p and p-on-n solar cells made by high beam current ion implantation will be competitive with the very best of today's diffused product.)

A second conclusion is that the open circuit voltage behaves as expected. Higher ion doses and lower sheet resistances in general tend to yield higher V_{OC} values. This is likely to be due to a simple "emitter efficiency" effect. Heavier doping in the emitter reduces the junction reverse saturation current and increases V_{OC}.

A third conclusion is that generation current (I_{gen}) tends to decrease with increased ion dose (and the consequently decreased sheet resistance). In some cases, such as the arsenic data of Figure 27, this effect is quite pronounced. There are several possible reasons for this. Higher dose and lower sheet resistance imply a deeper junction after annealing. Both the implanted impurity profile and impurity diffusion effects are responsible for junction depth increase. Deeper junctions can yield lower photogeneration current because of lost short wavelength response.

Moreover, too large an ion dose means that peak impurity concentration may exceed solid solubility. If C_p is the peak concentration in cm^{-3} of the implanted impurity profile, and ΔR_p is the range parameter of the implant (in cm), then the ion dose (N/A) in cm^{-2} is given as

$$N/A = \sqrt{2\pi}\,(\Delta R_p)\,C_p.$$

The solid solubility of arsenic in silicon at 900°C is approximately 10^{21} cm^{-3}. If this is to be the peak concentration, then a dose of $N/A = 5.5 \times 10^{15}$ cm^{-2} is required at an implant energy of 105 KeV. Hence, for doses greater than

5.5×10^{15} cm^{-2} there is a risk of exceeding solid solubility of arsenic. The comparable doses for boron and phosphorous at 105 KeV and 900°C are 4.7×10^{15} cm^{-2} and 7.2×10^{15} cm^{-2}, respectively. If solid solubility is exceeded, permanent lattice damage may result, electrically inactive dopant will be present, minority carrier lifetime will be degraded, and an appreciable so-called "dead-layer" may be formed which will result in reduced I_{gen}.

The empirical data trends of Figures 19 - 28 indicate that a trade-off is to be made between V_{OC} and I_{gen}. As V_{OC} is increased, I_{gen} may be reduced. This fact, along with solid solubility considerations, leads to the conclusion that the range of interest for further work should be narrowed to doses between 3×10^{14} cm^{-2} and 3×10^{15} cm^{-2} for smooth-surfaced solar cells. This would result in a range of sheet resistances between 30 and 200 Ω/□ for phosphorous, between 60 and 250 Ω/□ for boron, and between 50 and 250 Ω/□ for arsenic. These values are in agreement with reasonable diffused solar cell fabrication parameters as well.

The data discussed above are for bare, smooth-surface silicon. If a textured surface is considered, then doses greater by a factor of 1.73 will be needed to suppy the same dopant per unit area, since the textured surface area is effectively 1.73 times as great as a smooth surface. Since the ion beam must enter the <111> textured surface facet at an appreciable angle, the resulting junction will be shallower than for a smooth <100> test wafer. These geometrical effects of a textured surface have been widely discussed. In any case, a higher implant energy must be used to obtain the same junction depth on a textured surface as that of a polished surface. Furthermore, if the implant is to be performed through an antireflective dielectric coating on the silicon surface, then additional energy will be needed to penetrate the dielectric layer.

3.5.3 IMPLANTS THROUGH SILICON NITRIDE

When implanting into bare silicon surfaces, changes in implant energy will affect the implanted depth of the Gaussian impurity distribution, but all of the impurity dose will be within the silicon surface. This is not necessarily true when implanting through a dielectric layer, such as silicon nitride, which may have been applied to the silicon surface before implant. In this situation, some of the implanted ions will be stopped (and trapped) in the nitride layer. The amount of dopant incorporated in the dielectric layer depends on the energy of the implant, the effective thickness of the dielectric, and the stopping power of the dielectric. Silicon nitride deposited by low pressure CVD techniques has been determined to have approximately the same stopping power as silicon. That is, at a given implant energy, ions will penetrate low pressure CVD nitride to about the same depth as they would penetrate into bare silicon.

To allow for the stopping power of silicon nitride on a textured surface, a greater implant energy must be used than would be required for a bare textured surface. For example, consider a (100) silicon substrate with a 750Å thick silicon nitride (Si_3N_4) coating uniformly covering the textured front surface. An ion beam implanted perpendicular to the substrate would strike the (111) facets of the textured surface at an angle of 54.74°. Therefore, the effective thickness of the Si_3N_4 layer would be equal to 750Å/cos (54.74°) or 1300Å. Thus, the implanted ions must penetrate to a depth of 1300Å before they reach the silicon surface. If the implanted species is phosphorus, an energy of 105 KeV is required to place the peak of the Gaussian impurity profile at the Si_3N_4-Si interface. If the peak impurity concentration is at that interface, half of the ion dose will be in the silicon and the other

half will have been stopped and left in the nitride. Thus, effectively, only half of the applied dose is used. If an energy greater than 105 KeV is used, more dose will be placed in the silicon than in the nitride.

To extend the tests previously reported for polished surfaces and to determine the implant requirements for textured surface solar cells, two types of experiments have been performed on 1 Ω-cm p-type substrates. In one case, ion implanted solar cells were fabricated by implanting phosphorus into a bare, textured front and boron into a bare, smooth back. The phosphorus implant (P^{31}) was done at 35 KeV for three different doses: 8.4×10^{14} cm^{-2}, 1.74×10^{15} cm^{-2}, and 3.48×10^{15} cm^{-2}. These doses will form N-type surface layers equivalent in sheet resistances to those formed at 5×10^{14} cm^{-2}, 1×10^{15} cm^{-2}, and 2×10^{15} cm^{-2} on smooth silicon surfaces. The boron implant (B^{11}) was done at 40 KeV and 1×10^{15} cm^{-2}.

In the second case, phosphorus was implanted into a textured front surface covered with silicon nitride, and boron was implanted into a smooth back surface coated with nitride. The Si_3N_4 was about 600Å thick, giving an effective thickness of about 1390Å for the phosphorus to penetrate. The phosphorus implant was done at 140 KeV for the same doses as in the first experiment (the bare surface textured case). Since some of the implanted dose would be stopped in the nitride, leaving less doping in the silicon, sheet resistances should be higher for this experiment. The boron implant was done at 70 KeV with a 1×10^{15} cm^{-2} dose.

For both experiments, the implanted cells were annealed at 900°C for 30 minutes in N_2 with 2% O_2. The cells with silicon nitride were then etched to remove the dielectric. Both sets of bare silicon solar cells were electrically measured to obtain open circuit voltage and photogeneration

current for one sun illumination. Four point probe measurements were also made to determine the sheet resistance of the phosphorus junctions. These data are tabulated in Table 6 along with similar data for a control group of cells fabricated by boron and phosphorus gaseous diffusion techniques (BCl_3 and PH_3 were used). This control group is listed in Table 6 as group C. The cells with bare surfaces during implant are group B, while the cells coated with Si_3N_4 during implant are group A.

Three observations can be made concerning the data of Table 6. First, open circuit voltage (V_{OC}) depends primarily on phosphorus doping level since V_{OC} increases directly with decreasing sheet resistance. Second, cells implanted with bare silicon surfaces (group B) are significantly better than those implanted through the Si_3N_4 layer (group A). The reason for this has not been determined, but may be due to the possible differences in impurity profiles between A and B. Third, the control cells have larger voltages but smaller generation currents than those of group B. In fact, the implanted cells of group B could have greater output power (after metallization) than the controls of group C since, as phosphorus dose is reduced, generation current is increasing faster than open circuit voltage is decreasing.

3.5.4 EFFECTS OF ANNEALING CYCLE

Another variable of ion implantation is the effect of the annealing cycle following implantation. A variety of cycles have been utilized, both at Motorola and elsewhere in the industry. Agreement on an optimum cycle for annealing is still unresolved. During this contract, both single step and double step anneals have been investigated.

TABLE 6

TEST CELLS WITH TEXTURED FRONT SURFACE (PHOSPHORUS DOPED), SMOOTH BACK SURFACE (BORON DOPED), MEASURED BARE, WITH NO METAL CONTACTS.

	DOSE INTO TEXTURED SURFACE (cm^{-2})	SHEET RESISTANCE ρ_s ($\Omega/\square$)	OPEN CIRCUIT VOLTAGE V_{OC} (mV)	GENERATION CURRENT I_{gen} (mA)
A	8.7×10^{14}	305	530	1270
	1.74×10^{15}	164	543	1280
	3.48×10^{15}	82.0	556	1190
B	8.7×10^{14}	117	543	1490
	1.74×10^{15}	94.8	555	1390
	3.48×10^{15}	53.8	563	1310
C	---	47.4	576	1310

A Ion implanted through A.R. Nitride @ 140 KeV measured bare

B Ion implanted bare @ 35 KeV measured bare

C Phosphine diffused, measured bare

3.5.4.1 MULTIPLE STEP ANNEALS

Acomparison between a multiple step anneal cycle and a simple anneal at 900^{o} was performed. A group of 20 wafers (0.6 to 1.4 Ω-cm, <100>, p-type, bare, polished on one side) was fabricated into test solar cells by implanting the polished front with P^{31} for front junction formation at a dose of 3×10^{15} cm^{-2} at 35 KeV and implanting the back with B^{11} at a dose of 1×10^{16} cm^{-2} at 35 KeV for BSF and contact enhancement. After implant the lot was split in two. One half was annealed at 900^{o}C for 30 minutes in nitrogen with 2% oxygen. The other half was given a 2 hour soak at 550^{o}C before ramping up (for 20 minutes) to 900^{o}C and then being held at 900^{o}C for 30 minutes. This was also done in nitrogen and oxygen. After the anneal, all cells were coated with a silicon nitride antireflective coating using a low pressure CVD furnace. The polished front sides were then patterned with a metal contact grid pattern and the cell backs were stripped of dielectric. At this point the cells were electrically tested to determine solar cell performance.

Open circuit voltage, V_{OC}, and photogeneration current, I_{gen}, were measured for each half group of test cells. No significant difference was found between the two groups. The first group (900^{o}C only) had an average V_{OC} of 591 mV (with 6 mV standard deviation) and an average I_{gen} of 1483 mA (with 44 mA standard deviation). The second group (550^{o}C and then 900^{o}C) had an average V_{OC} 590 mV (with 3 mV standard deviation) and an average I_{gen} of 1477 mA (with 29 mA standard deviation).

No apparent performance advantage was seen, thus, for the only multiple step cycle attempted.

3.5.4.2 SINGLE STEP ANNEALING CYCLES

Investigations have been performed on the single step annealing of damage introduced by phosphorus ion implantation into bare wafers. Isochronal anneals of 30 minutes have been performed at different temperatures and for different implant doses.

The results of isochronal (30 minutes) anneals at temperatures ranging from 700°C to 950°C in 50°C intervals are presented in Table 7. For this data, phosphorus was implanted at a constant dose of 1×10^{15} cm^{-2} at 35 KeV into smooth (100) wafers at a 0° angle. The data show that, within experimental error, similar results have been obtained for anneals at all temperatures for the measured parameters of sheet resistivity, junction depth, generation current, and open circuit voltage.

Further annealing experiments were performed at two temperatures, 900°C and 735°C, for three different implant doses, 5×10^{14} cm^{-2}, 1×10^{15} cm^{-2}, and 2×10^{15} cm^{-2}. Data from these experiments, performed on higher resistivity material, are presented in Table 8. In this case, obvious effects of annealing temperature can be seen in both sheet resistivity and junction depth. Higher annealing temperatures give lower sheet resistivities, probably reflecting solid solubility effects. On the other hand, higher doses annealed at 735°C give consistantly lower junction depth, the opposite of expectations. This may be related to reordering of the damaged layer during annealing, the greater dose resulting in more rapid recrystallization due to the greater energy of the more heavily damaged material. Further studies will be performed The essentially constant junction depth for the 900°C anneals indicate that diffusion at that temperature is probably the dominant factor in determining junction depth. Again, however, little statistical difference is seen for generation current and open circuit voltage when comparing the two annealing temperatures.

TABLE 7: ANNEALING OF PHOSPHORUS IMPLANTS FOR 30 MINUTES AT VARIOUS TEMPERAUTRES. SMOOTH, BARE CZOCHRALSKI WAFERS (100), p-TYPE, 0.8 - 1.2 ohm-cm. IMPLANT AT 35 KeV, 0° ANGLE, $1 \times 10^{15}/cm^2$.

ANNEAL TEMPERATURE ($^{\circ}C$)	SHEET RESISTIVITY ($\Omega/\square$)	JUNCTION DEPTH (μm)	I_{gen} (mA)	V_{oc} (mV)
$950^{\circ}C$	82	0.55	1140	565
$900^{\circ}C$	89	0.5	1160	560
$850^{\circ}C$	90	0.55	1150	560
$800^{\circ}C$	91	0.55	1170	565
$750^{\circ}C$	92	0.55	1160	555
$700^{\circ}C$	89	0.5	1150	560

TABLE 8: ANNEALING OF PHOSPHORUS IMPLANTS FOR 30 MINUTES AT 900°C OR 735°C. SMOOTH, BARE CZHCHRALSKI WAFERS (100), p-TYPE, 2-5 ohm-cm. IMPLANT AT 35 KeV, 0° ANGLE.

IMPLANT DOSE (cm^{-2})	ANNEAL TEMPERATURE (°C)	SHEET RESISTIVITY (Ω/□)	JUNCTION DEPTH (μm)	I_{gen} (mA)	V_{oc} (mV)
5×10^{14}	900	170	0.5	1320	545
	735	190	0.45	1310	535
1×10^{15}	900	89	0.55	1310	550
	735	92	0.4	1310	535
2×10^{15}	900	48	0.5	1240	535
	735	65	0.35	1320	540

3.5.5 ION IMPLANT AND ACTIVATION ANNEAL STATUS

Implants have been performed for several dopant species at different doses and energies. This cost-effectiveness of implanting appears to be optimized at doses near 10^{15} cm^{-3} and at low implant voltages. Multi-step cycles, recommended in the literature, appear to give no advantage over simpler cycles. While trends have been established, a precise specification for optimum cost/performance effectiveness has not yet been ascertained. This is due to the complex interactions between dopant species, implant energy, implant dose, and annealing cycle. Further efforts are needed to define these interactions and establish the necessary process controls.

4.6 INCORPORATION OF METALLIZATION ADVANCEMENTS FROM PARALLEL STUDY

PALLADIUM-NICKEL-SOLDER METALLIZATION SYSTEM

Supported in part by funding from DOE/JPL Contract No. 954689, a metal plating sequence was developed to allow selective applications of metal contacts to all exposed silicon on solar cell surfaces. This metallization was incorporated into this Phase 2 study as part of the overall process sequence. The metallization includes both immersion and electroless palladium plating, heat treatment to form Pd_2Si, electroless nickel plating, and a subsequent solder coating. The application is selective in that metal is applied, in additive fashion, only to those cell areas on which metal is desired, eliminating the need for any subsequent metal removal or wastage.

The basic process sequence for applying the palladium-nickel-solder metallization system with selective plating techniques is listed below.

1. Immersion palladium coat (displacement reaction)
2. Heat treatment (silicide formation)
3. Electroless palladium plate (autocatalytic reaction)
4. Heat treatment (additional silicide formation)
5. Electroless nickel plate (autocatalytic reaction)
6. Solder coat

Many variations of this process sequence have been studied, but the steps listed above have given the most repeatable application of this metal system. Temperatures between 300°C and 700°C have been used for the heat treatment steps.

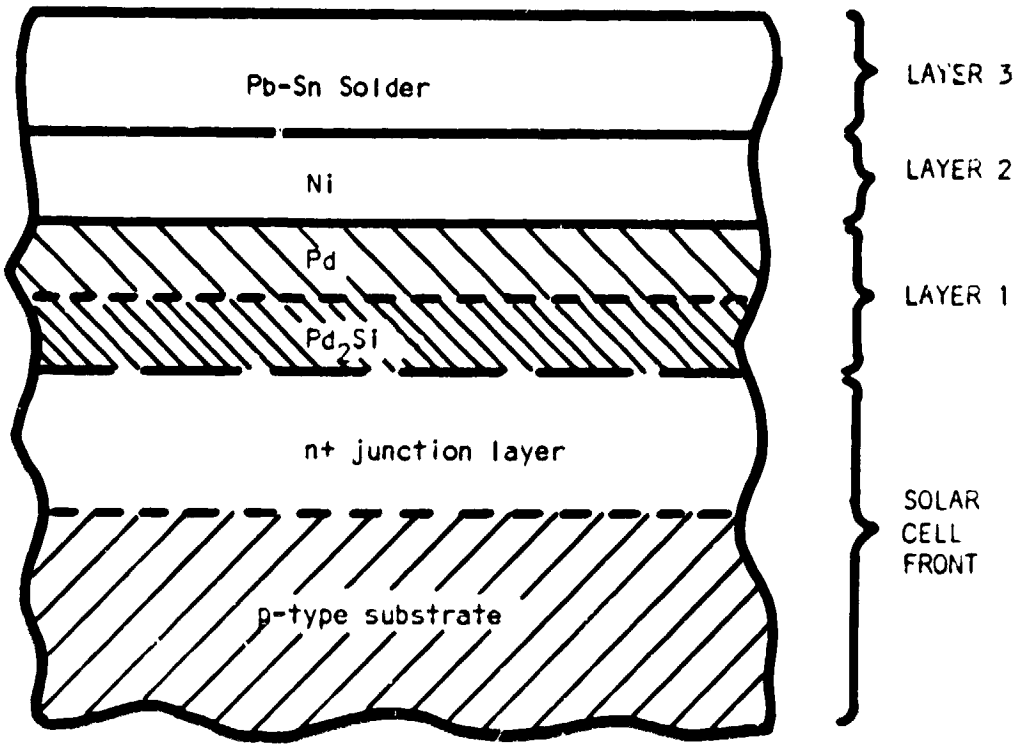


FIGURE 29: SCHEMATIC DIAGRAM OF PALLADIUM-NICKEL-SOLDER METALLIZATION SYSTEM, SHOWN FOR FRONT OF n-on-p SILICON SOLAR CELL.

As diagrammed in Figure 29 the completed metallization system consists of three layers upon the silicon substrate: a palladium silicide/palladium first layer, a nickel second layer, and a lead-tin solder third layer. Since front and back cell contacts are formed simultaneously, the metal system on the back surface is the same as that on the front surface.

The first layer of palladium silicide (Pd_2Si) is formed by heat treating the plated palladium layer. (The palladium may or may not be reacted completely.) The Pd_2Si serves as an adherent, ohmic contact to the silicon. The Pd layer can be heat treated at moderate temperatures to form the Pd_2Si without fear of rapidly degrading shallow junction solar cell characteristics. The silicide formation is responsible for the excellent adhesion of the metal system. In principal this layer can be very thin. In practice, the palladium layer has produced the most reliable results when plated to thicknesses (before reaction to form Pd_2Si) between 500Å and 1000Å.

The second layer of nickel provides a solderable metal surface which protects the palladium layer against rapid dissolution in molten lead-tin solder. The nickel itself dissolves very slowly in solder. Nickel layer thicknesses as great as 5000Å have been used. Obviously, the longer the nickel layer must withstand molten solder during solder coating and interconnection reflow operations, the thicker this layer must be.

The third layer of lead-tin solder provides the required high electrical conductivity while still utilizing a low cost metal. Moreover, solder is known to provide an additional degree of protection against ingressed moisture and contaminants from the terrestrial environment. Typically, 60 Sn/40 Pb solder has been used, although other solders are applicable.

In the development of this system, emphasis was placed on metal adhesion and the ability of the metal system to withstand high temperature solder reflow operations during cell interconnection. The only acceptable mode of contact adhesion failure is facture of the silicon substrate beneath the contact.

To apply this metallization, three chemical plating baths are employed. Palladium is deposited first with an immersion solution and then in an electroless bath; nickel is subsequently deposited with an electroless solution. Advances in the immersion palladium bath chemistry have resulted in a much improved immersion palladium deposition.

Until recently, the state-of-the-art immersion palladium solutions produced palladium deposits as reported in Quarterly Technical Report No. 1 for JPL Contract No. 954689; scanning Electron Microscope (SEM) photographs of a typical deposit of this type on a silicon surface are shown in Figure 30 for an immersion palladium solution prepared with water, fluoboric acid, hydrochloric acid, and palladium chloride, Table 9. The formation of a discontinuous granular clumps of palladium, and perhaps palladium salts*, is typical of this solution (and many others). Such a palladium deposit is not very adherent until it has been heat treated, presumably forming palladium silicide (Pd_2Si). Even then, much non-adherent material can be removed upon mechanical or hydraulic scrubbing. This loose material is probably palladium and palladium salts from the tops of the granular clumps. Furthermore, during electroless

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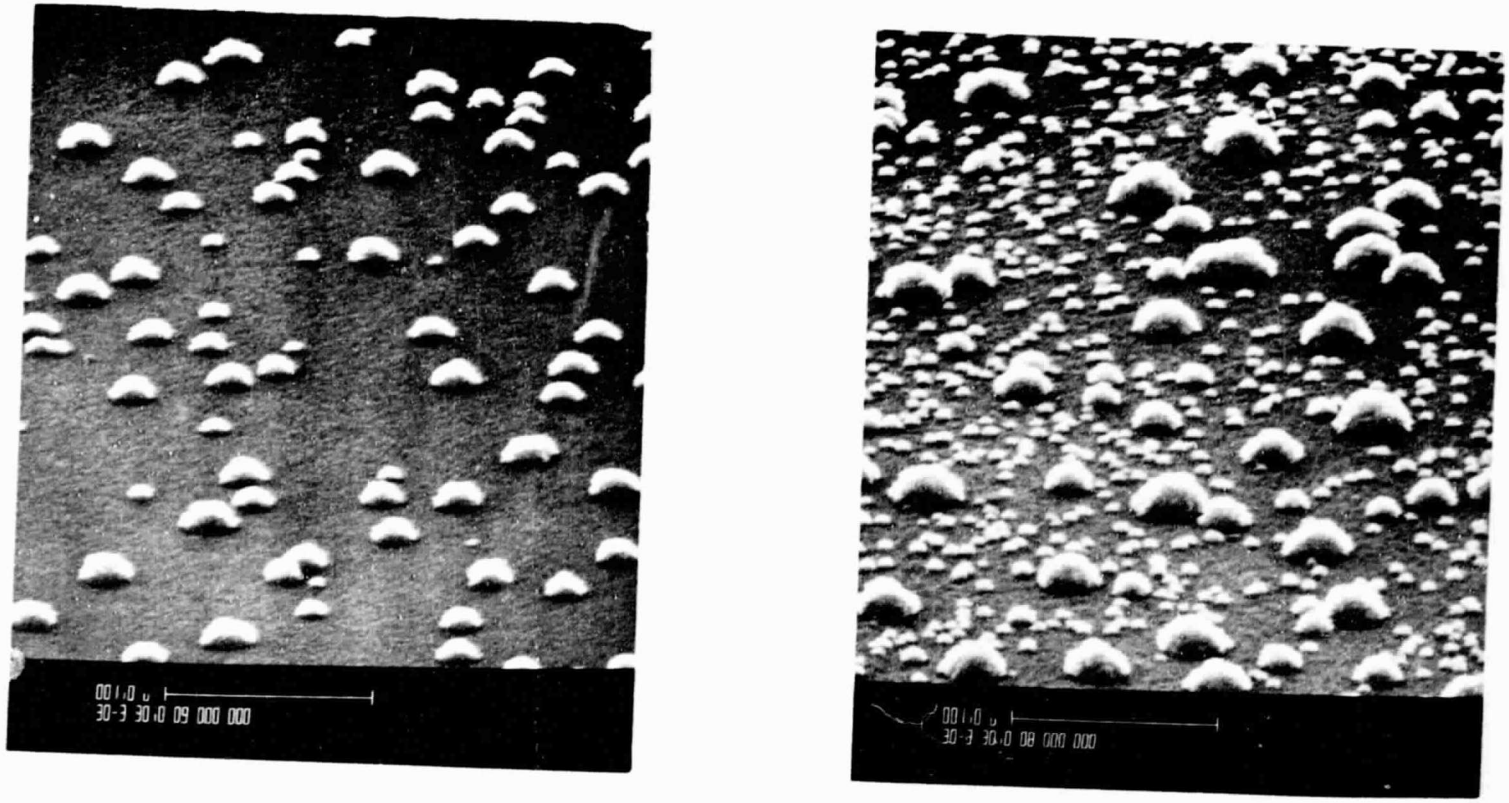
*During sintering of the immersion palladium layer, a metallic-looking deposit gradually built up on the quartz furnace tube. This deposit was analyzed as silicon. The most satisfactory explanation for how it got there involves halogen (chlorine) transport of silicon from the heated silicon waters to the cooler furnace wall. A possible conclusion is that at least part of the deposited film was palladium chloride.



(a) 75 sec. immersion

(b) 150 sec. immersion

FIGURE 30: IMMERSION PALLADIUM PLATING WITH FLUOBORIC ACID SOLUTION

TABLE 9

IMMERSION PALLADIUM SOLUTION

CONSTITUENT		AMOUNT
Water	H_2O	1000 mℓ
Ammonium Fluoride	NH_4F	67 mℓ
Hydrochloric Acid	HCl (38%)	3 mℓ
Palladium Chloride	$PdCl_2$	0.027 g

palladium deposition, the initiation of plating will occur preferentially at the clumps, and may not form intimately on the silicon surface area between the clumps. This is obviously not the most desirable plated film topography, and could result in a non-uniform palladium silicide layer formation even after electroless plating. Consequently, reduced adhesive strength was sometimes obtained between the silicon surface and the metal contact layers.

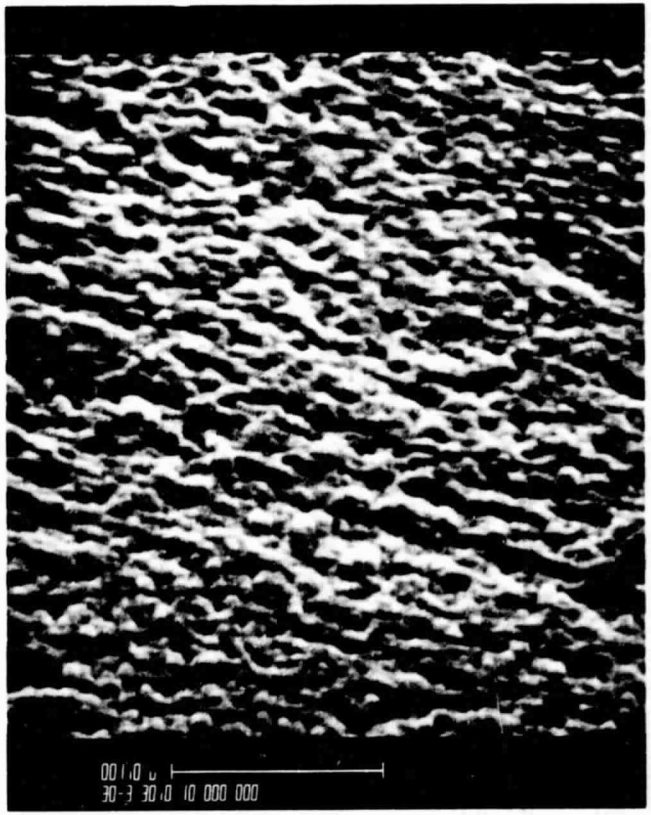
Figure 31 shows SEM photographs of a palladium layer deposited with a newly developed immersion palladium solution. In this case, a continuous layer of palladium** has been formed on the silicon surface. Such a layer could be capable of satisfying the requirements for formation of a very adherent layer of Pd_2Si.

The new immersion palladium solution eliminates the fluoboric acid (HBF_4) in favor of a low concentration of ammonium fluoride (NH_4F). The other constituents are water, palladium chloride ($PdCl_2$), and hydrochloric acid (HCl). This solution plates a thin metallic immersion layer with little or no loose palladium. The immersion layer will withstand a vigorous mechanical scrub and will consistently initiate adherent electroless plating.

The new plating chemistry is being incorporated into the overall process sequence being developed under this contract. An improvement in yield of highly adherent metal, and thus in the long term reliability of solar cells, is expected. Since the immersion layer is now completely continuous, it is possible that the electroless layer can be thinned, reducing the cost of this metallization to a value which is easily consistent with processing costs budgeted for a less than 50¢/watt solar cell module.

**Deposits of silicon do not appear on the quartz furnace tube when immersion palladium layers deposited by the new chemistry are sintered. This suggests that the film contains little or no chlorine (e.g. no palladium chloride).

(a) N+ front textured surface showing large Pd grains on top of continuous, fine-grained Pd layer.



(b) P+ back smooth surface showing continuous, fine-grained Pd layer.

FIGURE 31: IMMERSION PALLADIUM PLATING FROM AMMONIUM FLUORIDE TYPE IMMERSION PALLADIUM SOLUTION.

Formulation of the electroless palladium solution is given in Table 10. The electroless plating reaction is autocatalytic, which allows the palladium deposition to continue at a constant rate. Thus, a palladium layer can be deposited to any desired thickness. In this way, a reasonably thick and totally continuous layer of palladium is formed in process step 4. This ensures that a strongly adherent palladium silicide interface can be formed in step 5. One result of using sodium hypophosphite as a reducing agent for the electroless palladium solution is that the deposited palladium layer contains a small percentage (about 1% to 5%) of phosphorous.

Formulation of the electroless nickel solution is given in Table 11. The behavior of this electroless nickel bath is quite similar to that of the electroless palladium bath. Once again, nickel layer thickness can be increased as desired, and the deposited nickel layer contains a small percentage (3% to 15%) of phosphorus. Enough nickel is deposited in process step 6 to ensure that the subsequent soldering step will not allow molten lead-tin solder to dissolve the entire thickness of the nickel layer.

Following nickel plating, the cell metallization is completed by solder coating, presently performed by solder dipping.

The incorporation of two types of palladium plating baths into the NPMS process has resulted from empirical studies dedicated to defining a reproducible, economical process. Plating of a thin palladium layer onto the silicon surface from an immersion bath has proven to be a prerequisite for uniform and adherent plating from the electroless palladium bath. The immersion deposited layer should, in fact, be completely sufficient for both uniform palladium silicide formation and for subsequent plating from an electroless nickel bath, the next layer in the NPMS.

Elimination of the electroless palladium layer from the metallization has been studied under the parallel contract, with variable results on contact adherence. In the best cases, adherence was excellent -- as good as the best strengths obtained by any process. In other trials, however, contact adherence was reduced. At this point in time, exact reasons for this variability are undefined. Adherence may require a finite thickness of palladium between the palladium silicide and the nickel layers. Alternatively, surface stoichiometry of the palladium silicide formed from the thin immersion palladium layer may be silicon rich, allowing formation of an interfacial silicon oxide layer. In any case, feasibility of eliminating the electroless palladium layer has been demonstrated, but adequate process control requires further work. The elimination of this step and the attendant drying and sintering steps can effect a significant process simplification and cost reduction.

3.7 PROCESS SEQUENCE ENHANCEMENT

Synergistic interactions between various process steps within the process sequence can produce improvements in the overall sequence cost-effectiveness. During the course of this contract, several such interactions have been identified.

TABLE 10

ELECTROLESS PALLADIUM SOLUTION(*)

CONSTITUENT		AMOUNT
Water	H_2O	830 mℓ
Hydrochloric Acid	HCl (38%)	4 mℓ
Palladium Chloride	$PdCl_2$	2 g
Ammonium Chloride	NH_4Cl	27 g
Sodium Hypophosphite	$NaH_2PO_2.2H_2O$	3.75 g
Ammonium Hydroxide	NH_4OH (58%)	160 mℓ

(*) I. Pearlstein and R. F. Weightman, "Electroless Palladium Deposition", Plating, 56, 1158-1161 (1969).

TABLE 11

ELECTROLESS NICKEL SOLUTION(*)

CONSTITUENT		AMOUNT
Water	H_2O	875 mℓ
Nickel Chloride	$NiCl_2.6H_2O$	30 g
Ammonium Chloride	NH_4Cl	50 g
Sodium Citrate	$Na_3C_6H_5O_7.2H_2O$	84 g
Sodium Hypophosphite	$NaH_2PO_2.2H_2O$	10 g
Ammonium Hydroxide	NH_4OH (58%)	125 mℓ

(*) F. A. Lowenheim, Ed., Modern Electroplating, John Wiley & Sons, Inc., New York, 1974.

3.7.1 SMALL TEXTURE ETCHED PEAKS

The utilization of a textured front surface on a silicon solar cell has been shown to increase solar cell efficiency. This increase is a direct result of less reflection of light from the cell surface. The textured surface is comprised of a continuous field of pyramids; the base of each pyramid is a (100) plane, while the faces of the pyramids are (111) planes. Light incident normal to the plane of the substrate (and the plane of the pyramid bases) is either refracted into the silicon or is reflected directly onto an adjacent pyramid face. Reflected light, thus, is given a second incidence on the silicon surface. The geometries and effects of such textured surfaces have been widely discussed.

The formation of pyramidally textured silicon surfaces is achieved by means of any one of several anisotropic etchants. These may be formulated from several compounds known to etch silicon, such as various ammoniacal compounds and amines, hydrazine, or alkali hydroxides. These compounds display the ability to dissolve crystalline silicon at different rates depending on the direction of dissolution through the crystal lattice. By proper choice of etchant, directional preference, and crystal orientation, an etchant that produces the desired pyramidal surface can be specified.

The choice of etchant is limited by considerations in addition to etching efficiency. The amines and ammoniacal compounds pose problems of toxicity and availability, as well as those of odor and volatility. The extreme toxic nature of hydrazine is well documented. Hydrazine also possesses chemical reactivity that precludes its use; it reacts explosively with some of the commonly used cell processing reagents, raising problems associated with storage and contamination. The preferred etchants are those based on the plentiful and inexpensive alkali hydroxides. These compounds are easily stored and

present less of a health hazard than many of the acids presently used in cell manufacture. In addition, the alkali hydroxides have been thoroughly researched as to chemical and biological behavior and seem least likely to be the objects of government-regulated use in the future.

The etch now in use consists of an aqueous solution of any of the available alkali hydroxides along with various abundant commercially available organic compounds, which moderate the etching power of the hydroxide and increase the directional nature of its attack on silicon. In order to increase the speed of dissolution, the etchant composition is customarily used at elevated temperatures of from 50°C to 100°C. At these temperatures, the etchant produces the desired fully textured surface in 30 to 65 minutes.

From optical considerations, the size and distribution of the pyramidal peaks is unimportant. Light is reflected and refracted from large peaks, small peaks, or a mixture of large and small peaks is an identical manner. In terms of processing convenience, however, control of pyramid height is desirable. Large pyramids can cause problems in the masking and metallization processes used. Further, isolated large peaks, surrounded by a field of smaller pyramids present small, high areas that are very susceptible to damage from handling; depending on where they are and when in the process sequence the damage occurs, the effects can be appreciable on solar cell performance.

Several techniques have been discussed in the industry for controlling peak size. These, in general, require special treatment of the silicon surface or require special mechanical constraints during etching to initiate and maintain the desired peak size. We have found that peak size can be controlled solely by varying the composition and temperature of the texture-etch solution, eliminating the need for any special silicon treatment or external mechanical fixtures that may be required by other texture etching conditions.

The etchant composition used is easily prepared and has been characterized as to the effects of temperature and composition. As an advantage, spent etchant can be replenished -- apparently for an appreciable length of time -- by the addition of controlled amounts of fresh hydroxide, thus assuring minimal waste of consumed material.

This improved control of peak size by texture etching is being incorporated into the process sequence under development. The results are expected to be improved control and process yield, concomitant with low (and perhaps reduced) cost.

3.7.2 TEXTURE ETCHING OF AS-SAWED WAFERS

A process simplification which can have a major effect on equipment design for plasma etching of silicon has been identified. This process simplification requires the texture etching of the as-sawed surface on one side of the silicon wafer.

As discussed in Technical Quarterly Report No. 3 for this contract, the size of the peaks of a textured surface can have a major impact on the control and yield of the overall process. Small peaks are highly preferable; large peaks and broadly distributed peak sizes create problems for process control and peak breakage.

Early work at Motorola on texture etching of as-sawed wafers produced a broad distribution of peak sizes, and included some very large isolated peaks. These wafers were cut by an I.D. sawing technique. On the other hand, texture etching of wafers chemically etched to remove sawing damage produced a much more uniform distribution of peak sizes. Accordingly, it was deemed important to remove sawing damage prior to texture etching.

Two recent observations have indicated that the earlier conclusions can be changed. First, as reported in Technical Quarterly Report No. 3, the size of peaks can be controlled by modification in the composition of the texture etching solution. Second, wafers cut by wire sawing have significantly less depth of sawing damage (approximately a factor of two) than wafers cut by I.D. sawing. In combination, the size and size distribution of peaks resulting from texturing wire-sawed wafers with the new texture etch compositions can be acceptable without prior removal of the sawing damage.

If thin wafers, (near 100 microns or less) are utilized in cell manufacturing, optical considerations for maximizing cell efficiency dictate a smooth back surface and a textured front surface. The process sequence developed on this contract incorporates these features. The smooth back surface is achieved through removal of the sawing damage in a plasma silicon etching step.

Plasma silicon etching for sawing damage removal can be simplified if satisfactory texture etching can be performed directly on the as-sawed surface. Plasma etching would, thus, be required only on one side of the wafer. Actually, plasma etching of silicon is difficult to achieve at the points where the wafer is supported in the plasma chamber. Utilizing this effect, if etching of one side is not required, wafers can be placed either flat or back-to back in the plasma system. The simplification over requiring uniform etching on all surfaces of the wafer is appreciable.

3.7.3 ROUNDED VS. SHARP PEAKS FROM TEXTURE ETCHING

As has been reported by a variety of companies and by JPL, texture etching developed at Motorola (and some other firms) results in very well

defined, sharp peaks which have (111) crystalline faces. Peaks of similar shape, but which have rounded peaks and edges as well as "pillow-shaped" peaks, have also been reported.

Peaks which have well defined crystalline surfaces with no rounding are optically superior for light absorption to peaks which are rounded. In general, however, such well defined peaks require longer etching times (to develop the desired shape) than peaks which are rounded. There is, thus, an economic trade-off between sharply defined and rounded textured peaks. The cell with sharp peaks will have a higher efficency (due to increased light absorption), but will cost more (due to longer processing times) than the cell with rounded peaks. The net difference will be small. Quantitative evaluation of this trade-off will be most meaningful on very thin cells, not widely available now. Further, any change should have only a small impact on the process sequence. Accordingly, this comparison is left to a future study.

3.7.4 COMBINED ACTIVATION ANNEAL AND SILICON NITRIDE DEPOSITION

Ion implantation annealing at temperatures between 700°C and 750°C can allow a significant process simplification. The anneal can be performed within the same cycle as deposition of the silicon nitride layer, which is also performed in the 700° to 750°C range. This modification in the process sequence requires that the implant be performed into a bare surface.

Ion implantation through a dielectric requires a greater energy than implantation into a bare surface. Further, since some of the ion dose is stopped within the dielectric, a greater total dose must be delivered when implanting through a dielectric compared to a bare surface to achieve the same dose within the silicon. Implanting into a bare surface, thus, can increase the

throughput of an ion implanter. The lower voltage required for implantation into a bare surface can also result in equipment simplification for the ion implanter itself.

Implanting into bare silicon surfaces and combining the implant anneal with the silicon nitride deposition cycle can result in significant cost advantages, reducing the projected costs for an ion implantation process sequence.

3.8 COST ANALYSIS OF THE PHASE 2 PROCESS SEQUENCE

In addition to the SAMICS cost analysis, we have performed a cost analysis of the process sequence developed on this (Phase II) program, modelled after the cost analysis performed as part of the Phase I program (JPL Contract #944363) and covered in detail in the final report. By this comparison, a direct measure of the specific improvements to be gained via the current process are illustrated. This section presents pertinent assumptions and results of the cost analysis.

3.8.1 DETAILED PROCESS SEQUENCE

The detailed process sequence, including all cleaning, drying, and testing steps, is listed below:

1. Plasma silicon etch* (all surfaces)
2. Masking wax application (back surface)
3. Texture etch front surface
4. Wax removal
5. Plasma clean
6. Ion implant p-type **
7. Ion implant n-type **
8. Implant activation anneal ** ***
9. Silicon nitride deposition (all surfaces) ** ***
10. Plasma silicon nitride patterning **
11. Plating etch
12. Immersion palladium A
13. Spin dry (centrifuge)
14. Sinter

15. Immersion palladium B (flash) ****
16. Electroless palladium ****
17. Spin dry (centrifuge) ****
18. Sinter ****
19. Electroless Nickel
20. Spin dry (centrifuge)
21. Solder coat
22. Cell test
23. Cell Interconnect
24. Module clean
25. Module assembly, welding
26. Module cure
27. Module test

* May not be necessary with certain sheet materials.

** There are trade-offs for this portion of the process sequence, varying the exact order of these steps. The re-arrangement of the steps will, however, have minimal effect on this cost analysis.

*** May be combined into single step, eliminating cost of activation anneal.

**** May be eliminated in the future, contributing a major cost reduction.

3.8.2 GENERAL INPUTS AND ASSUMPTIONS

The Phase ! costing study assumed essentially current technology levels, and was applicable to a 1982 time-frame factory. For process steps in this sequence, the present study for comparative purposes also assumes current technology. As a result, automation is not incorporated

in this study; all that is required is that the process steps be automatable. Since automation advances can be assumed to be significant by 1986, the results of this study for the Phase II process sequence projects a very conservative cost, i.e., an upper cost limit for the specified process sequence.

At the present time, the form of the starting silicon substrates in 1986 is an unknown. Accordingly, this cost analysis assumes that the process starts with a prepared substrate. The cost of the process, thus, is a value-added cost over and above the cost of the starting substrates.

Further general assumptions are as follows:

1. The factory produces only one product and supplies less than ten customers.
2. Annual production level: 100 megawatts (20% of total market)
3. Solar cell efficiency: 14% encapsulated (15% bare).
4. Insolation: 1 kilowatt/M^2 (peak).
5. Wafer diameter: 12.0 cm.
6. Only one module type fabricated in the factory.
7. Total work days/year = 240, (260 - 20, vacation, holidays, etc.)

3.8.2.1 MATERIALS AND EXPENSE ASSUMPTIONS

The costs, in mid-1977 dollars, and sizes of specific items utilized in this analysis are listed below:

MATERIALS

Polycrystalline Silicon	-	$11.70/kg (10.00/kg in 1975 dollars).
Cold Rolled Steel	-	$0.225/lb (0.020 inch thick), $0.204/lb (0.030 inch thick), based on 99% yield and density of 7.83 g/cm^3.

Nylon Coating	-	0.003 inch powder coating at $0.0225/mil/ft^2.
Glass	-	3/16 inch clear tempered glass at $10.91/4 ft. x 4 ft. sheet, 99% yield (incoming).
Silicone	-	0.009 inch thick, $3.75/lb (in 800 lb. drums) at 8 lbs/ gallon.
Polysulfide gasket	-	$0.60 (based on $6/gallon).
Interconnect	-	$0.60/ft^2, 99% yield (incoming)
Feedthroughs	-	$0.60, (2 at $0.30 each).
D.I. WATER		
Volume Rate	-	$0.0031/gal.
ELECTRICITY		
Power rate	-	$0.025/kilowatt-hour
ACIDS		
Hydrochloric	-	$2.97/Gal.
Buffered Hydrofluoric	-	$2.95/Gal.
Waste Treatment	-	$0.0020/Gal. X DIH_2O consumption
SOLVENTS		
Deionized Water (DIH_2O)	-	$0.0031/Gal.
GASES		
Nitrogen	-	$ 0.0033/CF
Argon	-	$ 0.1172/CF
Oxygen	-	$ 0.002/CF
PH_3	-	$28.0702/CF
Hydrogen	-	$ 0.044/CF
H_2SiCl_2	-	$ 8.6331/CF
NH_3	-	$ 1.0619/CF

SOLUTIONS

Nickel Plating	-	$ 0.48/liter
Palladium Plating	-	$ 2.137/liter
Texture Etching	-	$ 2.38/Gal.

IMPLANT SOURCES

Enriched Boron	-	$200/lb.
Phosphorous	-	$ 2.76/gram

3.8.2.2 DIRECT LABOR ASSUMPTIONS

A number of assumptions are made for direct labor, many of which are also utilized for indirect labor. As discussed later in the overhead assumptions, however, each labor category has its own salary assumption.

1. One work day = 3 shifts = 22.5 work hours; (24-1.5 lunch)
2. First shift, second shift, third shift - 8, 8, 6.5 hrs. respectively
3. Second and third shift premium = 10%
4. First shift salary rate = $4.00/hour
   (Rate with burden and fringes = $5.96/hour)
5. Absentee/turnover time loss factor = 5%
6. Miscellaneous laboratory supplies (paper towels, record forms, pencils, etc.), protective clothing, and safety equipment are assumed to be $325/year for each direct labor employee.

3.8.2.3 BUILDING, DEPRECIATION, AND INTEREST ASSUMPTIONS

Assumptions utilized in determining building, depreciation, and interest costs are listed below:

1. Construction cost for production space is $80/sq. ft.
2. Construction cost for support space is $30/sq. ft.
3. Depreciation on building: Straight line for 40 years.
4. Depreciation on manufacturing equipment: Straight line over life of factory, starting after equipment is installed.
5. Depreciation on support equipment: Straight line for eight years.
6. Interest rate: 10%

3.8.2.4 PROCESS STEP AND EQUIPMENT SPECIFICATIONS AND ASSUMPTIONS

This section defines the equipment specifications and asumptions for each process step utilized in all of the process sequences. Since the number of individual process steps is large, a common format is utilized for consistency. Each step is numbered for identity in the final costing data. The format utilized is as follows:

CAPITAL EQUIPMENT ASSUMPTIONS

- Type of equipment (Manufacturers model where possible)*
- Cost of equipment
- Maximum capacity of equipment (showing calculations)
- Floor space requirements (equipment and aisle and work area)
- Labor requirement

EXPENSE ITEMS

- Equipment facility requirements (electrical, exhaust, water, gases, etc.)
- Chemical and material consumption (showing calculations)
- Parts used on equipment requiring periodic replacement

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*The specification of a given manufacturer does not necessarily mean that Motorola would prefer that manufacturer or equipment item over a competitive product. In most cases, competitive equipment exists and may be comparable or superior. Identification in this report, however, allows substantiation of information and allows direct comparison with other possible choices to determine suitability of the cost assumptions with those of other cost analysis studies.

- Non capitalized items necessary to perform the process (e.g., furnace tubes, beakers, etc.)

MATERIAL ITEMS

- Items appearing in finished product, (e.g., silicon, metal, module parts).

STEP 1: PLASMA SILICON ETCH

Capital Equipment Assumptions

This process assumes an RF plasma unit which contains two separate vacuum chambers, each capable of processing two 50 wafer carriers. One chamber will process wafers while the other is being loaded. A complete cycle will be 10 minutes including chamber evacuation, etch, and vent. It is assumed, by utilization of a $CF_4 + O_2$ gas, that an etch rate of 2 μ/min can be achieved. Thus, to remove a 12 μ layer from each side of the substrate, an active etch time of six minutes is necessary. Using the 10 minute cycle time figure and the 100 wafer/load figure, 600 wafers can be processed each hour. Equipment requirements include $15K capital cost, 30 ft^2 per machine, and 0.5 direct labor personnel per machine.

EXPENSE ITEMS

Electrical	1.5 KW
Exhaust	40 CFM
Vacuum pump oil	$418/year/machine

Process gas is calculated as follows:

- 1A cylinder of CF_4 = 70 lbs (31.75 Kg)
- specific volume = 4.4 ft^3/lb (0.27 m^3/Kg)
- cost = $1260/cylinder

. $\frac{31.75\ Kg}{cylinder} \times \frac{0.27\ m^3}{Kg} \times \frac{10^6 cm^3}{m^3} = \frac{8.5725 \times 10^6\ cm^3}{cylinder}$

. @ flow of 750 cm^3/min => $1.143 \times 10^4 \frac{min}{cylinder}$

. @ six minutes/ run = $1.905 \times 10^3 \frac{runs}{cylinder}$

$\therefore \frac{\$1260}{cylinder} \times \frac{1\ cylinder}{1.905 \times 10^3\ runs} \times \frac{1\ run}{100\ wafers} = \frac{\$6.61}{1000\ wafers}$

STEP 2: WAX APPLY

Capital Equipment Assumptions

Equipment utilized in this process step is assumed to be similar to that used to coat wafers with photoresist, and to bake the photoresist layers. In this equipment, wafers will be pre-heated in a belt drive IR oven, transported to a heated chuck and coated with molten wax. This equipment consists of four separate tracks, each capable of processing 250 wafers per hour, a cabinet, and a laminar flow hood and represents a capital expenditure of $58,960. Necessary manufacturing area is 80 ft^2 and 0.5 operators are required for each machine.

EXPENSE ITEMS

Facility requirements are:

Electrical	1.1 KW + 2.5 KW/track
Exhaust	120 CFM/track

An additional expense item is the net cost of the wax used to coat the wafers; this will be largely saved by recycling, so a 1% utilization factor is employed.

. wax layer thickness = 0.02"

. wax density = 0.78 g/cm^3

. wax cost = $0.59/lb = $1.30/Kg

$$\frac{12\ cm^2 \times \pi}{4} \times 0.02" \times \frac{2.54\ cm}{in} \times \frac{0.78\ g}{cm^3} = 4.48\ g/wafer.$$

@ 10% wax used:

$$\frac{4.48g}{wafer} \times \frac{\$1.30}{Kg} \times 0.01 = \frac{\$0.06}{1000\ wafers}\ (wax)$$

STEP 3: TEXTURE ETCH

Capital Equipment Assumptions

Equipment used in the texture etch process includes a six foot laminar flow exhaust hood (IAS LV - 30X) containing six etch tanks (7" wide x 6" deep x 20" long) and a chemical recirculating system (Fluorocarbon Model 5000) which is used to maintain the etch integrity. The cost of the hood is $4500 and the recirculating system costs $7500 resulting in a total system cost of $12K. Assuming a one hour process time:

$$\frac{50\ wafers}{carrier} \times \frac{3\ carriers}{sink} \times \frac{6\ sinks}{hood} = \frac{900\ wafers}{hour}$$

Floor space is 45 ft^2 and one operator is necessary for two such hoods.

EXPENSE ITEMS

Facility requirements include:

Electrical	1.6 KW
Exhaust	500 CFM

Assumptions used in the cost analysis for chemicals are as follows:

Displacement of carrier and 50 wafers is 515 cm^3.

Assuming a liquid level of 6" when three loaded carriers are placed in the tank, then:

$$\left(\frac{1375\ cm^3}{tank} \times \frac{515\ cm^3}{carrier}\right) \times \left(\frac{3\ carriers}{tank}\right) \times \frac{6\ tanks}{hood} \times \frac{2.64 \times 10^{-4}\ gal}{cm^3} = \frac{19.3567\ gal.}{hood}$$

$$\frac{19.3567\ gal}{hood} \times \frac{\$2.3783}{gal.} \times \frac{60}{year} = \frac{\$2762}{year}\ (chemical\ costs)\ per\ hood$$

$= \frac{\$0.57}{1000 \text{ wafers}}$ if the equipment is fully utilized.

Additional expense items include:

Carriers:

$$2 \times \frac{3 \text{ carriers}}{\text{sink}} \times \frac{6 \text{ sinks}}{\text{hood}} \times \frac{\$32.00}{\text{carrier}} = \$1152.00/\text{year per hood}$$

= $0.24/1000 wafers if fully utilized.

Quartzware: Assume $\$1/in^2$ for quartz liners which results in

$$\frac{464 \text{ in}^2}{\text{liner}} \times \frac{6 \text{ liners}}{\text{hood}} \times \frac{\$1}{\text{in}^2} = \$2784/\text{hood}$$

These liners should have a two year life resulting in $1392/year cost. The liner cost is thus $0.27/1000 wafers assuming 100% equipment utilization.

STEP 4: WAX REMOVAL

Capital Equipment Assumptions

This process step assumes a piece of equipment similar to a high pressure scrubber as described in Step 6. This equipment removes wax by spraying high pressure steam over the wax-coated substrate, thus removing the wax, and reclaiming it with a 99% efficiency. A four track unit is assumed to cost $56,495, process 1000 wafers per unit (250/track), require 45 ft^2 of floor space and one operator.

EXPENSE ITEMS

Electrical	1.1 KW + 0.25 KW/track
Exhaust	80 CFM/track
DIH_2O	0.8 GPM/track

STEP 5: PLASMA CLEAN

Capital Equipment Assumptions

It is anticipated that a two chamber unit, each chamber capable of containing two 50 wafer carriers, will be used. A complete cycle will be 15 minutes including pump down, ash, and vent. Since only one chamber can be operated with rf power at a time, the other will be vented, unloaded, loaded, and pumped down and waiting for the 10 minute ashing cycle. Thus, six runs/hour X 100 wafers/run result in a throughput of 600 wafers/hour. It is expected that a plasma asher of this type can be bought for $15K. Floor space is 30 ft^2 and one operator can run two units.

EXPENSE ITEMS

Electrical 1.5 KW

Exhaust 40 CFM

Vacuum pump oil @ $\frac{\$17.42}{\text{bottle}} \times \frac{24 \text{ bottles}}{\text{year}} = \frac{\$418.08}{\text{year}} = \frac{\$0.13}{1000 \text{ wafers}}$,

assuming 100% utilization of the equipment.

STEPS 6 AND 7: ADVANCED ION IMPLANTATION

This system will use an unanalyzed ion beam system. Current cost and capacity estimates anticipate that a 100 mA phosphorus system and a 10 mA boron system can be purchased for $85K. Utilizing a belt transport system through a differentially pumped vacuum chamber, implant times will probably be mechanically limited to 0.5 sec/wafer. The chart below shows estimated implant times and throughputs.

	Calculated time (sec)	Machine time (sec)	Throughput (WPH)
Phosphorus (2×10^{15} @ 100 mA)	.6696	.75	4800
Boron (1×10^{15} @ 10 mA)	3.348	3.5	1030
Boron (8×10^{14} @ 10 mA)	2.6784	2.75	1310

Floor space is assumed to be 400 ft^2 and one operator is required for each implanter.

EXPENSE ITEMS

Electrical	50 KW
Exhaust	40 CFM
DIH_2O	10 GPM

Expense items for LN_2, vacuum pump oil, and ion sources are calculated to be $265/year, $1.94/1000 wafers and $0.3659/1000 wafers reqpectively.

STEP 8: ACTIVATION ANNEAL

Capital Equipment Assumptions

This process step assumed a Thermco eight-tube diffusion module Type 4000S72 per Spec 19000 with load station, source cabinets and appropriate options at $49,271. Process controllers are estimated to be $2,000/tube resulting in a total system cost of $64,271.

One operator will run the system, assuming a one hour average process time. Using the close pack (50 wafer) dump transfer type boat, 250 wafers/tube or 2000 wafers/hour can be processed. Floor space required for this diffusion system is 275 ft^2.

EXPENSE ITEMS

Facility requirements are:

Electrical	140 KW per module
Exhaust	125 CFM per module
N_2	3 ℓ/min. per tube

$$\frac{3\ \ell}{min} \times \frac{60\ min}{hr} \times \frac{.0353\ CF}{\ell} \times \frac{5400\ hr}{year} \times \frac{\$.0033}{CF} = \$113.25/year\ per\ tube$$

Quartzware: (assume tubes and boats replaced annually) = $769/year per tube

H_2 and Quartzware, thus, represent $0.084 and $0.57, respectively, per 1000 wafers assuming 100% utilization of the equipment.

STEP 9: SILICON NITRIDE DEPOSITION

Capital Equipment Assumptions

This process step utilizes a Thermco eight-tube diffusion module, Type 4000S72 per Spec 19000 with load station, source cabinets and appropriate options at $49,271. Process controllers estimated to be $2,000/tube result in a total system cost of $65,271.

One operator will run the system, assuming a one hour average process time. Using the close pack (50 wafer) dump transfer type boat, 250 wafers/tube, or 2000 wafers/hour, can be processed. Floor space required for this system is 275 ft^2.

EXPENSE ITEMS

Facility requirements are:

Electrical	140 KW
Exhaust	125 CFM

Gases used in the formation of this dielectric anti-reflection layer are shown below:

H_2SiCl_2: $\frac{10\ cm^3}{min} \times \frac{60\ min}{hr} \times \frac{5400\ hr}{year} \times \frac{3.53 \times 10^{-5}\ CF}{cm^3} \times \frac{\$8.6331}{CF} = \frac{\$987.50}{year}$

NH_3: $\frac{15\ cm^3}{min} \times \frac{60\ min}{hr} \times \frac{5400\ hr}{year} \times \frac{3.53 \times 10^{-5}\ CF}{cm^3} \times \frac{\$1.0619}{CF} = \frac{\$181.25}{year}$

Assuming that this equipment is 100% utilized, H_2SiCl_2 and NH_3 represent costs of $0.73/1000 wafers and $0.13/1000 wafers, respectively.

Quartzware: (assume tubes and boats replaced annually) = $769/year per tube = $0.57/1000 wafers, assuming 100% utilization of the equipment.

STEP 10: PLASMA SILICON NITRIDE PATTERNING

Capital Equipment Assumptions

The patterning of silicon nitride is performed in a parallel plate RF plasma etching chamber. In this chamber, twenty 12 cm diameter wafers are aligned on a carrier and placed between two metal plates containing the ppropriate patterns. The assembly is placed into the vacuum chamber, pumped down, interlock transferred into the etching chamber, etched, transferred through an interlock, and vented. Assuming a 15 second load, 2 minute pump down, 2 minute etch (while next load is pumped down), 30 second vent (while next load is etched), 15 second unload, a total of 2.5 minutes are required to perform the etch process, resulting in 480 cells per hour. Capital for this item is $65K, floor space is 100 ft^2, and there is one operator per machine.

Expense Items

Electrical	10.5 KW
Exhaust	40 CFM

CF_4

$$\frac{300\ cm^3}{hr.} \times \frac{1\ hr.}{480\ wafers} \times \frac{\$1260}{cylinder} \times \frac{1\ cylinder}{8.5725 \times 10^6\ cm^3}$$

= $0.0735/1000 wafers

Vacuum pump oil = $418/yr/machine

STEP 11: PLATING ETCH

Capital Equipment Assumptions

This step is a preparation to remove any SiO_2 layer existing prior to metallization. A six foot laminar flow exhaust hood is used at a 1977 cost of $4500. The hood is assumed to have six etch tanks, rinse tanks (or sinks) each 7 inches wide by 6 inches deep by 20 inches long. In this application, there will be three etch tanks and three rinse tanks. Each tank can hold 3 carriers of fifty 12 cm wafers. The cycle for etching and rinsing one carrier of wafers is 15 minutes, allowing 1800 wafers/hr. The hood and work space occupy 45 ft^2. One operator is required.

Expense Items

Electrical	1.6 KW
Exhaust	500 CFM
DIH_2O	3 GPM
Chemicals	$1380/year
Hardware	$1968/year

STEP 12: IMMERSION PALLADIUM COAT AND WATER RINSE

EQUIPMENT This step assumes the same six foot laminar flow exhaust hood and set-up as in the previous step (Step 11) with the addition of a chemical recirculating system (such as Fluorocarbon Model 5000). The chemical recirculating system is used to agitate the immersion palladium plating bath and to pump plating solution from the working tanks through a reservoir where the condition of the solution can be monitored and the solution can be replenished. The addition of the recirculating system adds a cost of $7500 for a total 1977 cost of $12,000.

Again wafers are handled in 50 wafer cassettes and a cycle time of 15 minutes is assumed. Thus, there are 4 cycles/hr. This gives maximum throughputs per hood identical to Step 11. Floor space and operator requirements are also identical to those described in step 11.

Expense Items

Electrical	1.6 KW
Exhaust	500 CFM
Chemicals	260.38/yr
DIH_2O	3 GPM

Material Items

Palladium costs are computed independent of the solution costs. Palladium is introduced in the bath as palladium chloride ($PdCl_2$) which has a 1978 cost of 1.66 per gram, translating to a 1977 cost of $2.766 per gram of palladium. For the purpose of this analysis, it is assumed that an effective layer of 50Å of palladium is applied. For a density of 12.16 g/cm^3, this requires a weight of 6.08×10^{-6} g per cm^2 of metallized surface area. Thus, assuming 7% coverage of the front and 14% coverage of the back, 23.75 cm^2 are covered. This coverage represents a materials cost of $0.3994/1000 wafers.

STEPS 13, 17, and 20: SPIN DRY (CENTRIFUGE)

Capital Equipment Assumptions

Cost estimates are based on the use of a Fluoroware K-100 rinser-dryer. This apparatus will hold four 25 wafer cassettes and cost $2500. A 15 minute cycle time (including load and unload) will be assumed, resulting in a throughput of:

$$\frac{25 \text{ wafers}}{\text{cassette}} \times \frac{4 \text{ cassettes}}{\text{machine}} \times \frac{4 \text{ runs}}{\text{hour}} = \frac{400 \text{ wafers}}{\text{machine-hour}}$$

Floor space required for this equipment is estimated to be 30 ft^2. One operator will run four units.

EXPENSE ITEMS

Facility requirements include:

Electrical	1 KW (115 VAC - 8.5 A)
N_2	13.2 ℓ/min @ 40 psi

Assume two wafer carriers for each slot in the cradle, one in use and one being loaded or unloaded.

8 carriers x \$32.00/carrier = \$256.00/machine

STEPS 14 and 18: SINTER

Capital Equipment Assumptions

Once the wafers are rinsed and dried, an anneal must be performed. The most probable cost effective method is to transport the wafers through a furnace on a continuous belt. Assume two carriers, each containing 50 wafers, are placed on a belt. Also, assume the time necessary for these carriers to pass through the furnace is 30 minutes and that two new boats of wafers can be placed on the belt every 30 seconds. After the first 30 minutes, two boats containing a total of 100 wafers will emerge every 30 seconds. This results in a throughput of 200 wafers/minute = 12,000/hour. For this process step, a belt furnace costing \$35K and requiring 132 ft^2 is assumed. Each furnace will require an operator.

EXPENSE ITEMS

Electrical	15 KW
Exhaust	100 CFM
N_2	50 ℓ/min = \$1888/year

STEP 15: IMMERSION PALLADIUM (FLASH)

Capital Equipment Assumptions

Equipment used in this step is identical to that used in the previous immersion palladium step (Step 12). All assumption are the same as in Step 12.

Expense Items

As in the equipment assumptions, expenses will be identical to those described in Step 12.

Material Item

In this process step, the immersion is performed for 15 seconds rather than 2 minutes. The amount of palladium plated onto the wafer, thus, is assumed to be 1/8 that plated onto the wafer in Step 12. Material cost will be $0.0499/1000 wafers

STEP 16: ELECTROLESS PALLADIUM

Capital Equipment Assumptions

The electroless palladium step is assumed to require the same equipment, labor, and expense items as have been described in the immersion palladium steps (Steps 12 and 15).

Material Items

Palladium solutions costs is $2.77/ℓ. It is assumed that the palladium content of the solution is used with 95% efficiency.

Materials costs are calculated for a palladium layer thickness of 800Å and an effective density of 11.98 g/cm^3. This density is slightly less than the density of elemental palladium. This assumption is made

because the electroless palladium layer actually contains a small percentage of phosphorus. The amount of palladium available per liter is

$$\frac{2 \text{ g } PdCL_2}{\ell} \times \frac{106 \text{ g Pd}}{177.306 \text{ g } PdCl_2} \times 0.95 = \frac{1.140 \text{ g Pd}}{\ell}$$

Using the same 21% coverage as previously described, a volume of 1.9×10^{-4} cm^3 is required resulting in a cost of $6.2969/1000 wafers.

STEP 19: ELECTROLESS NICKEL

Capital Equipment Assumptions

This step assumes the same equipment (laminar flow exhaust hood and chemical recirculating system) used in previous metallizing steps but the cell throughput will be different. The wafers are handled in 50 wafer carriers and a cycle time of 20 minutes is assumed. Thus there are threee cycles/hour. This gives a maximum throughput of 1350 wafers/hr. All other equipment and expense assumptions remain the same.

Materials Items

Materials costs are calculated for a nickel layer thickness of 5000Å and an effective density of 7.77 g/cm^3. The amount of nickel available per liter is

$$\frac{30 \text{ g Ni Chloride}}{\ell} \times \frac{58.71 \text{ g Ni}}{237.71 \text{ g Ni Chloride}} \times 0.95 = \frac{7.039 \text{ g Ni}}{\ell}$$

Based on a solution cost of $0.4414/ℓ, nickel represents a cost of $0.1743/1000 wafers.

STEP 21: SOLDER COATING

Capital Equipment Assumptions

This process step assumes an automatic solder system which contains a flux applicator, pre-heater, solderer, and a cleaning and drying section.

Including a wafer transport system this apparatus is estimated to cost $50K. Other assumptions include:

- solder fountain width is 15"
- transport speed is 10 ft/min

Using these assumptions, three wafers can be processed simultaneously. If the wafers are transported with one diameter spacing, then:

$$\frac{12.7 \text{ wafers}}{\text{min}} \times 3 \text{ tracks} = \frac{38.1 \text{ wafers}}{\text{min}} = \frac{2286 \text{ wafers}}{\text{hour}} .$$

EXPENSE ITEMS

Facility requirements include:

Electrical	15 KW
Exhaust	4000 CFM
DIH_2O	10 GPM

Flux will coat 200 ft^2/gal = 185,806 cm^2/gal. Since both sides of the wafer must be totally fluxed, areas are 2X single side area. Therefore, 1643 wafers can be fluxed. At $10/gal:

$$\$10 \times \frac{1 \text{ gal}}{1643 \text{ wafers}} = \frac{\$6.09}{1000 \text{ wafers}}$$

MATERIAL ITEMS

Solder:

4.33/lb = $6.7745/1000 wafers (21% coverage).

STEP 22: ELECTRICAL TEST-CELLS

Capital Equipment Assumptions

This process step requires an automatic wafer transport system, cell alignment stage, data acquisition system, and illumination source. These items are estimated to cost:

. Wafer transport system	$20K
. Cell alignment stage	5K
. Data acquisition	16K
. Illumination source	1K
. Temperature controlled stage	4K
TOTAL	$46K

It is estimated that a cell can be tested in 5 seconds resulting in a throughput of 720 cells per hour. Floor space is 100 ft^2 and one operator is required for each cell test station.

EXPENSE ITEMS

Electrical	2 KW

STEPS 23, 24, 25, and 26 MODULE FABRICATION

Capital Equipment Assumptions

Equipment assumptions used in this analysis are, in many cases, based on equipment not yet developed. The procedure of panel assembly is listed below:

1. Cell align (aligns and attaches cells by reflow to interconnect substrate)
2. Clean (removes flux)
3. Assembly (places substrate with cells attached into pan, injects silicone, and places glass over cells)
4. Rivet/Weld (attaches bezel)
5. Cure (thermally cures silicone)

Using the process outlined above, the following equipment assumptions are made: (modules are a nominal 4 ft. square containing 99 solar cells).

1. Cell align - For this operation, the interconnect is attached to an indexing X-Y table. Cells are aligned for X, Y and θ and placed on the substrate. Using localized heating, the cell is attached at this time. Following each cell attachment, the X-Y table indexes and another cell is aligned and placed on the substrate. It is anticipated that, by using a hybrid of today's technology equipment, this step can be achieved in this manner. Estimated cost of such a machine is $80K. The area required for such a machine is expected to be 10' X 10'. Including support space, a total area of 200 ft^2 is necessary. Alignment time is assumed to be 5 seconds/cell resulting in a panel alignment time of 8.25 minutes for 12 cm diameter cells (99 cells X 5 sec./cell). Using a cassette fed system, one operator can handle this process step.

2. Clean - After cells are attached by solder reflow to the interconnect substrate, solder flux must be removed. For this process step, assume a belt transport system which will spray a cleaning agent. An aqueous flux is suggested such that the spray can be water. The floor space, throughput, and operator requirements are assumed to be 350 ft^2, 15 panels/hour based on a 5 foot wide belt moving at 1 ft/min., and one operator. Capital cost is estimated to be $35K.

3. Assembly - Cleaned interconnect substrates containing attached solar cells are placed into a pan assembly, covered with silicone from an injector apparatus, and have a glass cover plate put over the array. It is assumed that an automatic belt transport system can perform this process at the same rate as described above in a machine requiring 500 ft^2 costing $55K and requiring one operator.

4. Rivet/Weld - Assembled panels are indexed into an area where a bezel is placed over the panel after a peripheral sealant has been injected. Riveting occurs at a rate of 1 panel/minute = 60 panels per hour. This equipment is estimated to cost $50K, require 144 ft^2 and one operator.

5. Cure - The final process used in panel assembly is a temperature cure which requires 2 hours. Assume a 6' high oven which is loaded from a belt and will contain 24 panels (2"/panel + 1" space). If a panel can be inserted into the oven in 5 seconds, then 2 minutes are necessary to load the oven which can be included in the 2 hour cure time. Floor space is estimated to be 25 ft^2 (5' X 5") for the oven plus 400 ft^2 (20' X 20') for staging and loading apparatus plus 175 ft^2 for work area = 600 ft^2 total. It is estimated that the oven will cost $15K and the load apparatus $20K, for a total of $35K. One operator will be required.

EXPENSE ITEMS

Panel Assembly

Item	Cost (K$)	Area (ft^2)	Capacity (PPH)	Power (KW)	Exhaust (CFM)	DIH_2O (GPM)	N_2 (ℓ/m)	Staff (OPI)
Cell Align	80	200	5.91	1.5	--	--	--	1
Clean	35	350	15	1	400	10	25	1
Assembler	55	500	15	4	400	--	--	1
Riveter	50	144	60	2.5	--	--	--	1
Cure	35	600	12	200	200	--	--	1

MATERIAL ITEMS

Pan Requirements

- Size: 48" X 48" X .02" = 2304 in^2 X .02" = 46.08 in^3
- Material: Cold Rolled steel
- Bezel requirements, four pieces
  - 4 X 2.5" X 48" X .03" = 480 in^2 X .03" = 14.4 in^3

Item	Unit $	$/W
Pan	$ 3.2145	.0205
Bezel	0.8394	.0054
Coating	2.7937	.0178
Glass	11.0202	.0703
Feedthrough	.60	.0038
Insulator	.092	.0006
Interconnect	9.6970	.0619
Silicone	5.4857	.0350
Gasket	.60	.0040
TOTAL	$34.3425	.2191

STEP 27: ELECTRICAL TEST - MODULE

Capital Equipment Assumptions

Panel testing is assumed to use a Spectrolab LAPSS pulsed lamp system which costs $80K. Automatic indexing of panels into the test area is expected to add $15K to the equipment cost. A room 8' wide X 22' long is necessary for uniform illumination of a 4' X 4' panel. Additional area for the panel indexing system is expected to require that a total area of 250 ft^2 be provided for this process step. One operator is necessary for this equipment. 15 seconds will be allowed for this operation resulting in a 240 panel/hour rate.

EXPENSE ITEMS

Electrical 2.5 KW

3.8.2.5 OVERHEAD ASSUMPTIONS

The specific categories which contribute to overhead costs are presented in this secton. Each category is itemized; in no case is any category merely taken as a percentage of some quantity, such as labor. Specific categories are presented below:

Direct Factory Overhead

This section includes one foreman per shift and is independent of the range of factory sizes to be evaluated (a conservative assumption). Supervisors are required at one per 15 direct labor personnel in crystal and wafer processing areas and one per 25 direct labor personnel in the panel assembly area. Annual salaries are assumed to be $16K for foremen and $10K for supervisors. Direct factory expense items are listed in a separate expense category.

Engineering

The engineering area will maintain process integrity and perform Q.A. functions. The following engineering staff will remain constant over the range of annual producton to be evaluated.

(1) Manager @ $23K/year

(3) Engineers @ $20K/year each

(3) Technicians @ $280/week each

Capital equipment is expected to cost $185K and will be depreciated over 8 years on a straight line basis. Associated expenses are assumed to be 25% of the total engineering cost, excluding depreciation.

Production Control

Since this factory produces only one product and the number of customers will remain essentially constant, annual production volume will only minimally

effect this size of the production control operation. The following personnel will staff this area:

(1)	Manager	@ $22K/year
(1)	Secretary	@ $172/week
(1)	Scheduler	@ $18K/year
(2)	Clerks	@ $160/week
(1)	Customer Service Engr.	@ $18K/year
(1)	Order Entry Clerk	@ $172/week
(4)	Inventory Control	@ $174/week

This group will remain constant up to 5 MW annual production at which time one inventory control person will be added for each additional 5 MW of annual production. It is assumed that this group will provide warehouse personnel requirements. Capital equipment, depreciated as support equipment, will include fork-lifts, pallet trucks, and the storage racks. Expense items are assumed to be 5% of salaries.

Building Services

This cost category includes lighting and HVAC which are estimated to be 48¢/ft^2/month; taxes and insurance which are estimated to be 25.3¢/ft^2/month; and custodial services which are estimated to be 0.118 man/1000 ft^2 @ $180/week. The square footage of the facility is based on the following assumptions. The total area figure (TOTAL SQ. FT.) represents only that area which is used for direct manufacturing. In order to estimate the cost of the building as well as area related costs, an estimate of the total factory size must be made. These estimates assume:

TOTAL SQ. FT. X 1.3 = DFA (Direct Factory Area)

This additional 30% is included in the overall factory size to account for hallways and storage areas within the manufacturing area.

DFA X 1.2 = FTL (Factory Total)

It is assumed that an additonal 20% of the manufacturing area is required to warehouse a 30 day product inventory.

FTL X 1.3 = TBA (Total Building Area)

This additional 30% of the total factory area is utilized for all support functions.

The results of this division of area are:

49% = direct manufacturing area

15% = hallway and storage areas within the manufacturing area

13% = warehouse area

23% = support area

Construction costs are assumed to be $\$80/ft^2$ for manufacturing areas and \$30/ft for all other areas. The average cost to build a factory is then: .49 X ($\$80/ft^2$) + .51 X ($\$30/ft^2$) = $\$54.50/ft^2$. Two distinct factory areas are identified in this cost analysis. The first is direct manufacturing area which is determined by adding the areas required for each piece of equipment used in the several production areas. This manufacturing area represents 49% of the total factory area and, due to the high degree of utility facilitization, construction costs are estimated to be $\$80/ft^2$. The remaining, non-facilitized, support area (i.e., office, warehouse, etc.) represents 51% of the total factory area and can be constructed for an estimated $\$30/ft^2$. Using these ratios of construction costs and factory utilization, an average construction cost of $\$54.50/ft^2$ for the total factory area was determined. In this analysis, the method used to calculate total factory construction costs is to multiply the

area required for direct manufacturing by the average construction cost ($54.50) and divide by the percentage of area used for manufacturing (49%). This artificially allocates all of the construction costs to the direct manufacturing area for calculation purposes only, and therefor results in an effective construction cost of $111.20/ft^2 direct manufacturing area. The total construction cost of the factory, thus, is the product of this effective construction cost/ft^2 and the TOTAL SQ. FT.

The cost of industrial property varies significantly throughout the U.S. For example, Phoenix, Arizona has industrial property in the $12 - 15K/acre range while San Francisco sells similar property for $95 - 125K/acre. The national average is approximately $1/ft^2 or $44K/ acre. In order to achieve an average cost estimate for a solar cell manufacturing plant, $1/ft^2 will be used in this analysis. Furthermore, it will be assumed that the total area of the building will be 30% of the total property area. Since the manufacturing area (TSQFT) is 49% of the factory and the factory is 30% of the total property, the effective construction costs of $111.20/ft^2 of direct manufacturing space will be increased to include property by $6.80 resulting in an effective cost of $118/manufacturing ft^2. Area calculations are utilized in the building services costs. Factory building costs form the base for the interest and depreciation figures.

Maintenance

Assumptions here are that one administrator at $30K/year (1st shift only) and one supervisor at $20K/year per shift for each 10 technicians are employed. Mechanical/electrical technicians at $15K/year each are determined by the

number and type of equipment used. Each type of machine is designated a maintenance coefficient in the data file to determine maintenance technician requirements for a particular process. Expense items are assumed to be 1.5X technician total salary, and material items are assumed to be 1/3 of the total maintenance cost, (payroll + fringes + expense)/3.

Management

The management section of overhead is assumed to contain a general manager at $50K and four staff members at $30K each. Expenses are 20% of these salaries.

Marketing/Sales

Due to the small customer base, the staff in this group is assumed to remain constant and to comprise of one product marketer and one salesman, each with annual salaries of $20K, and one clerk at $172/week. Expenses are 1/2 of these salaries and commissions are 2.4 X salesman's salary. It is also assumed that there are no applications activities.

Purchasing

The purchasing function is assumed to remain constant with one purchasing agent at $22K/year and expenses of 20% of salary.

Finance

Finance personnel include on accounts payable clerk, one accounts receivable clerk, and one payroll clerk each at $172/week. Expenses are 20% of salaries. This function is assumed independent of volume.

Secretary Pool

Two secretaries and two clerks, each with salaries of $172/week, are assumed for this section. Expense items are assumed to exist in several areas in which these employees work.

Data Processing

This operation is constant and utilizes a leased computer and peripheral equipment at $3500/month. The computer will provide inventory tracking, direct labor reporting, reject analysis, and management information services. One programmer/operator at $20K is required. Expenses are assumed to be $10K per year.

Training

Training is considered to be one of the most important functions in the overhead section. As a result, one organizer at $22K, five trainees for wafer processing at $170/week, and one trainer for assembly at $170/week will be employed. These people perform an extensive training program for direct labor personnel. In both situations, expenses are assumed to be 10% of salaries.

Personnel

This section requires two employees at $22K for each 10 MW of annual production. Expenses are 10% of salaries. The manager for this section is included in the Management section.

Cafeteria

Equipment for the cafeteria is estimated to cost $60K. Assuming that the cafeteria is self-sustaining and operates at a breakeven point, no labor or expense need be included.

Legal

It is assumed that all legal matters will be performed by a contract attorney for $18K/year.

Security

Security guards will be employed on a one employee per shift basis at $170/week.

Health

Nurses will be hired on a one nurse per shift basis at $200/week. Expenses are 10% of salary.

Fringe Benefits

For all direct labor employees, fringe benefits are assumed to be $2.3K/year times the number of employees regardless of salary or grade.

3.8.2.6: PROCESS YIELD AND MACHINE EFFICIENCY ASSUMPTIONS

The cost of performing any given process step (and the entire process sequence) is, in addition to expenses already defined, heavily dependent upon the yield through each process step. The yield of a given process step is simply defined as the number of acceptable units out of the process step divided by the number of acceptable units started into the process step. If a process step has well defined control ranges and is operated within those ranges, the yield should be 1.00 (or 100%). Since some variations can always be expected outside the control limits (including breakage from handling), the practically observed yields are always less than 1.00. Based upon volume extrapolations from today's known technology, yields have been assumed for each of the individual process steps which could be incorporated into the factory under consideration.

The yield of the overall process sequence is merely the product of the yields of each of the individual process steps in the sequence. A poor yield

at any one process step, thus, can dramatically affect the total yield. Further, to obtain 100 units out of the process sequence, the number of units started must be 100 divided by the yield. This, of course, is also true for any individual process step or group of steps. All substrates which are started but which do not finish, thus, are wasted and have a great impact on the cost of a step (and the overall sequence). One of the most cost sensitive sets of assumptions is the set of process yield assumptions. Since these assumptions must be, in fact, estimated, they are more subjective than many of the other assumptions previously discussed. A careful evaluation of the results of this cost analysis must critically evaluate these yield assumptions.

A second set of assumptions which are partially subjective and which also are highly influential on processing costs are related to machine durability. In this analysis, it is assumed that each piece of processing equipment will be broken down and inoperative a certain portion of the time. It is further assumed that the more complex machinery will have more down-time. An ion implanter, therefore, will have significantly more down-time than a chemical exhaust hood.

The process step yield and machine efficiency assumptions are listed below.

	PROCESS YIELD %	MACHINE EFFICIENCY
1. Plasma Etch	99.80	.97
2. Wax Apply	99.40	.92
3. Texture Etch	99.20	.93
4. Wax Remove	99.60	.95
5. Plasma Clean	99.80	.97

		PROCESS YIELD %	MACHINE EFFICIENCY
6.	Ion implant p-type	99.8	.80
7.	Ion implant n-type	99.8	.80
8.	Implant activation anneal	99.4	.96
9.	Silicon nitride deposition	99.2	.88
10.	Plasma patterning	99.4	.90
11.	Plating etch	99.8	.93
12.	Immersion palladium A	99.8	.93
13.	Spin dry	99.8	.96
14.	Sinter	99.8	.96
15.	Immersion palladium B	99.8	.93
16.	Electroless palladium	99.4	.93
17.	Spin dry	99.8	.96
18.	Sinter	99.8	.96
19.	Electroless nickel	99.4	.93
20.	Spin dry	99.8	.96
21.	Solder coat	99.0	.88
22.	Cell Test	94.80	.95
23.	Cell Attach	99.70	.88
24.	Module Clean	99.90	.88
25.	Module Assembly, Rivet-Weld	99.95	.88
26.	Cure	99.95	.97
27.	Module Test	99.80	.95

3.8.2.7 ELECTRICAL AND DI WATER CONSUMPTION ASSUMPTIONS

Electrical consumption in the factory includes the requirements for operation of building services and equipment as well as the specific requirements for heating, ventilating, and air conditioning (HVAC) in each of the processing areas. The total electrical consumption assumes:

(1) Steady-state operation of equipment requires 50% of the name-plate power (a 50% load factor).

(2) Exhaust power is rated at 100% load factor based on 8766 hours per year.

(3) HVAC power is rated at 40% load factor, based on 8766 hours per year.

(4) Lighting requires 4 watts per square foot.

It is further assumed that:

(5) Exhaust power requirement is 0.46 KW/1000 CFM and is assumed to operate continuously.

(6) HVAC requirements must account for:

(a) Equipment heat dissipation equal to 12.5% of name-plate rating and

(b) conditioning of make-up air at 15 KW/1000 CFM.

DI water consumption assumes a 5400 hour work year. Total electrical and DI consumption for each equipment item and for the total factory can now be calculated utilizing these assumptions.

The consumption of electricity and DI water in the factory is dependent upon the particular building service or type of equipment and process step. Consumption can be classed either as continuous or as demand, and costs have been determined for each piece of equipment accordingly.

Many of the building services and pieces of equipment require full time usage of a particular service whether material is being processed or not. For this continuous usage, consumption is equal to the number of pieces of process equipment required, multiplied by both the individual equipment service requirement and the machine efficiency value (presented earlier in the equipment and process step assumptions). Those pieces of equipment that require the usage of a particular service only when material is being processed will use that service at a rate equal to the product of the machine utilization factor and, again, the product of the number of pieces of that equipment, the individual equipment service requirement, and the machine efficiency value. Demand electrical items are then multiplied by 0.616, (5400 work hours/year)/(8766 hours/year), in order that weekends and holidays can be eliminated in determining the total annual electrical consumption. It should be noted that the machine utilization is factored into electrical and DIH_2O consumption only; exhaust is assumed to operate continuously.

Once totals are established for each facility requirement in each process sequence, annual consumption is determined by multiplying the total by 8766 annual hours for electrical consumption and by 5400 annual work hours for DIH_2O consumption.

3.8.3 CALCULATIONS FOR THE COST ANALYSIS

Description of the calculations are given below.

Calculations for the Process Sequence Yield

The average hourly solar cell output volume required to meet any given annual production goal can be readily calculated when the solar cell size and efficiency are specified. This hourly number is that which would result from a process with a 100% process yield. Knowing the required output rate

and the individual process step yields, the number of solar cells started into any process sequence can be calculated from the cumulative yield of the individual process steps. (The cumulative yield at a given process step is the product of all the individual process step yields including and following that step.) An example of this calculation, for the Phase II process utilizing 12 cm diameter cells at an annual production of 25 megawatts, is shown in the first three columns of Table 12.

The key for the table is:

STEP YLD (%)	=	Step yield (%)
CUM YLD (%)	=	Cumulative Yield (%)
WAFERS PER HR	=	Wafers per hour
MACH EFF	=	Machine Efficiency
MACH CAP	=	Machine Capacity
YIELD CAP	=	Yielded Machine Capacity

Having defined both a machine capacity and a machine efficiency in the assumptions, a yielded machine capacity is calculated from the product of the capacity and efficiency. This information is shown in the last three columns of Table 12.

Calculations for Machine Cost, Labor, and Floor Space Requirements

Results of the previous calculations are used to calculate total equipment requirements from an actual number standpoint as well as capital cost and floor space requirements, Table 13. The equipment (machine) requirements in both decimal and rounded-up (actual) form are shown in this table to illustrate the effect of machine utilization. The actual number of

TABLE 12

PHASE II PROCESS — 12CM CELL CONFIGURATION
100.0 MEGA WATT ANNUAL PRODUCTION — 14.00 % CELL EFFICIENCY
SOLAR CONCENTRATION = 1 SOLAR CONSTANTS

PROCESS STEP	STEP YLD(%)	CUM YLD(%)	WAFERS PER HR	MACH EFF	MACH CAP	YIELD CAP
PLASMA ETCH	99.8	86.5	13522	.97	600	582
WAX APPLY	99.4	86.7	13493	.92	250	230
TEXTURE ETCH	99.2	87.2	13414	.93	900	837
WAX REMOVE	99.6	87.9	13307	.95	250	237
PLASMA CLEAN	99.8	88.2	13254	.97	600	582
ION IMPL-ADV P	99.8	88.4	13227	.80	1030	824
ION IMPL-ADV N	99.8	88.6	13201	.80	4800	3840
DRIVE-IN DIFF.	99.4	88.8	13174	.96	250	240
SILICON NITRIDE	99.2	89.3	13095	.88	250	220
PLASMA PATTERN	99.4	90.0	12991	.90	480	432
PLATING ETCH	99.8	90.6	12913	.93	1800	1674
IMMERSION PD A	99.8	90.8	12887	.93	1800	1674
SPIN DRY	99.8	90.9	12861	.96	400	384
SINTER 1	99.8	91.1	12835	.96	12000	11520
IMMERSION PD B	99.8	91.3	12810	.93	1800	1674
ELECTROLESS PD	99.4	91.5	12784	.93	1800	1674
SPIN DRY	99.8	92.0	12707	.96	400	384
SINTER 1	99.8	92.2	12682	.96	12000	11520
ELECTROLESS NI	99.4	92.4	12657	.93	1350	1256
SPIN DRY	99.8	93.0	12581	.96	400	384
SOLDER	99.0	93.1	12555	.88	2286	2012
CELL TEST	94.8	94.1	12430	.95	720	684
CELL ATTACH	99.7	99.3	11784	.88	720	634
MODULE CLEAN	99.9	99.6	11748	.88	1485	1307
MODULE ASSEMBLY	99.9	99.7	11736	.88	1485	1307
RIVET-WELD	99.9	99.7	11731	.88	5940	5227
CURE	99.9	99.8	11725	.97	1188	1152
MODULE TEST	99.8	99.8	11719	.95	23760	22572
FINISHED PRODUCT	100.0	100.0	11695			

TABLE 13

PHASE II PROCESS — 12CM CELL CONFIGURATION
100.0 MEGA WATT ANNUAL PRODUCTION — 14.00 % CELL EFFICIENCY
SOLAR CONCENTRATION = 1 SOLAR CONSTANTS

PROCESS STEP	#MACH (DEC)	#MACH (ACT)	K$ MACH	TOTAL K$	LABOR MACH	TOTAL DL	SQFT MACH	TOTAL SQFT
PLASMA ETCH	23.23	24	15.0	360	.50	12	30	720
WAX APPLY	58.67	59	59.1	873	.12	8	80	1200
TEXTURE ETCH	16.03	17	12.0	204	.50	9	45	765
WAX REMOVE	56.15	57	56.4	807	.25	15	45	675
PLASMA CLEAN	22.77	23	15.0	345	.50	12	30	690
ION IMPL-ADV P	16.05	17	85.0	1445	1.00	17	400	6800
ION IMPL-ADV N	3.44	4	85.0	340	1.00	4	400	1600
DRIVE-IN DIFF.	54.89	55	65.3	469	.12	8	275	1973
SILICON NITRIDE	59.52	60	65.3	512	.12	8	275	2153
PLASMA PATTERN	30.07	31	65.0	2015	1.00	31	100	3100
PLATING ETCH	7.71	8	4.5	36	1.00	8	45	360
IMMERSION PD A	7.70	8	12.0	96	1.00	8	45	360
SPIN DRY	33.49	34	2.5	85	.25	9	30	1020
SINTER 1	1.11	2	35.0	70	1.00	2	132	264
IMMERSION PD B	7.65	8	12.0	96	1.00	8	45	360
ELECTROLESS PD	7.64	8	12.0	96	1.00	8	45	360
SPIN DRY	33.09	34	2.5	85	.25	9	30	1020
SINTER 1	1.10	2	35.0	70	1.00	2	132	264
ELECTROLESS NI	10.08	11	12.0	132	1.00	11	45	495
SPIN DRY	32.76	33	2.5	82	.25	9	30	990
SOLDER	6.24	7	50.0	350	1.00	7	100	700
CELL TEST	18.17	19	46.0	874	1.00	19	100	1900
CELL ATTACH	18.59	19	80.0	1520	1.00	19	200	3800
MODULE CLEAN	8.99	9	35.0	315	1.00	9	350	3150
MODULE ASSEMBLY	8.98	9	55.0	495	1.00	9	500	4500
RIVET-WELD	2.24	3	50.0	150	1.00	3	144	432
CURE	10.18	11	35.0	385	1.00	11	600	6600
MODULE TEST	.52	1	95.0	95	1.00	1	250	250
TOTAL				12402		276		46501

machines required in a particular step is then multiplied by capital cost, labor requirements, and floor space requirements. Similar to the machine data, the labor also represents a rounded-up integer for each step. (Reduction in this one shift labor figure will occur in later calculations utilizing process grouping techniques.) Totals at the bottom of Table 13 show the cost of capital equipment necessary to fabricate product and the necessary floor space to perform this task.

The key for Table 13 is:

# MACH (DEC)	=	Number of machines in decimal form
# MACH (ACT)	=	Number of machines in rounded-up form
K$ MACH	=	Individual machine cost in $1000 units
TOTAL K$	=	Total cost of machines in $1000 units
LABOR MACH	=	Direct labor to operate one machine
TOTAL DL	=	Direct labor, rounded-up, to operate all machines
SQFT MACH	=	Individual machine floor space (ft^2)
TOTAL SQFT	=	Total machine floor space (ft^2)

Grouping of Labor Within Process Categories

The direct labor headcount for a single shift, shown in Table 14, is higher than necessary. It can be lowered by grouping processes together to more efficiently utilize available labor. This reduction reflects the fact that while an integral number of machines is necessary, only a fractional number of machines would be necessary to fulfill production requirements. These calculations are shown in Table 14.

TABLE 14

PHASE II PROCESS — 12CM CELL CONFIGURATION
100.0 MEGA WATT ANNUAL PRODUCTION — 14.00 % CELL EFFICIENCY
SOLAR CONCENTRATION = 1 SOLAR CONSTANTS

PROCESS GROUPING

PROCESS STEP	EQPT UTL (%)	LABOR UTL (%)	LABOR /STEP	LABOR (DEC)	LABOR (ACT)
WAFER PREP					
PLASMA ETCH	96.8	96.8	12	11.6	
WAX APPLY	99.4	91.7	8	7.3	
TEXTURE ETCH	94.3	89.0	9	8.0	
WAX REMOVE	98.5	93.6	15	14.0	
PLASMA CLEAN	99.0	94.9	12	11.4	
TOTAL			56	52.4	56
JCT/DIELECT FORM					
ION IMPL-ADV P	94.4	94.4	17	16.1	
ION IMPL-ADV N	85.9	85.9	4	3.4	
DRIVE-IN DIFF.	99.8	85.8	8	6.9	
SILICON NITRIDE	99.2	93.0	8	7.4	
TOTAL			37	33.8	36
METALLIZATION					
PLASMA PATTERN	97.0	97.0	31	30.1	
PLATING ETCH	96.4	96.4	8	7.7	
IMMERSION PD A	96.2	96.2	8	7.7	
SPIN DRY	98.5	93.0	9	8.4	
SINTER 1	55.7	55.7	2	1.1	
IMMERSION PD B	95.7	95.7	8	7.7	
ELECTROLESS PD	95.5	95.5	8	7.6	
SPIN DRY	97.3	91.9	9	8.3	
SINTER 1	55.0	55.0	2	1.1	
ELECTROLESS NI	91.6	91.6	11	10.1	
SPIN DRY	99.3	91.0	9	8.2	
SOLDER	89.1	89.1	7	6.2	
TOTAL			112	104.1	110
ASSEMBLY					
CELL TEST	95.6	95.6	19	18.2	
CELL ATTACH	97.8	97.8	19	18.6	
MODULE CLEAN	99.9	99.9	9	9.0	
MODULE ASSEMBLY	99.8	99.8	9	9.0	
RIVET-WELD	74.8	74.8	3	2.2	
CURE	92.5	92.5	11	10.2	
MODULE TEST	51.9	51.9	1	.5	
TOTAL			71	67.7	72
PROCESS TOTAL					274

The key for Table 14 is:

EQPT UTL (%)	=	Equipment Utilization (%)
LABOR UTL (%)	=	Labor Utilization (%)
LABOR/STEP	=	Labor per step
LABOR (DEC)	=	Direct labor represented in decimal form
LABOR (ACT)	=	Direct labor, next highest integer after factoring for absenteeism and turnover

Equipment utilization is the ratio of the decimal number of machines over the actual number of machines and represents the percentage of time (after factoring of maintenance time) a particular item must operate in order to produce the desired volume. Labor utilization is determined by multiplying the actual number of machines required for a particular step by the labor per machine figure (which was identified in the assumptions) and dividing by the integerized direct labor value from Table 14. Using the assumption that the number of direct labor personnel specified for a particular process step can perform that operation when the equipment is 100% utilized, then the actual labor utilization figure, listed in Table 14, is the product of the figure calculated above and machine utilization. For each process step, the decimal labor requirement is determined by multiplying the labor per step figure from Table by the labor utilization figure in Table 14. To determine the actual direct labor required in a particular process category, the sum of all the individual process steps (decimal labor) within that particular category are multiplied by 1.05 to account for a 5% absentee/turnover rate and rounded up to the next highest integer. The purpose of listing labor

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requirements in both decimal and rounded-up form is to determine if sufficient personnel exist within a process category to perform the miscellaneous tasks not directly related to the manufacturing of product. Note that equipment utilization should not be confused with the actual percentage of time that a particular piece of equipment is used, but that it represents the percentage of available time that the piece of equipment is used; available time being total time reduced by maintenance, cleaning, and any other time in which equipment cannot be used.

Facility Requirement Calculations

Facility requirements are calculated for each process step and for the process sequence utilizing the requirements for individual pieces of equipment. The facilities necessary to perform each process step are shown in Table 15.

The key for Table 15 is:

PWR KW (1st)	=	Maximum rated (name-plate) electrical power in kilowatts for one machine.
VENT CFM	=	Exhaust in cubic feet per minute for one machine
WTR GPM	=	Deionized water in gallons per minute for one machine
# MACH	=	Number of machines required for the process step
PWR KW (2nd)	=	Electrical power in kilowatts for the number of machines in the step (includes machine efficiency, utilization and demand, but not 50% load factor)

TABLE 15

PHASE II PROCESS — 12CM CELL CONFIGURATION
100.0 MEGA WATT ANNUAL PRODUCTION — 14.00 % CELL EFFICIENCY
SOLAR CONCENTRATION = 1 SOLAR CONSTANTS

	IND EQPT FACILITY REQ				PROCESS STEP FACILITY REQ				
PROCESS STEP	PWR KW	VENT CFM	WTR GPM	# MACH	PWR KW	VENT CFM	WTR GPM	MACH EFF	EQPT UTL%
PLASMA ETCH	1	40	.0	24	20	931	0	.97	96.8
WAX APPLY	11	480	.0	59	163	6513	0	.92	99.4
TEXTURE ETCH	1	500	.0	17	25	7905	0	.93	94.3
WAX REMOVE	2	320	3.2	57	30	4331	45	.95	98.5
PLASMA CLEAN	1	40	.0	23	20	892	0	.97	99.0
ION IMPL-ADV P	50	40	10.0	17	395	544	128	.80	94.4
ION IMPL-ADV N	50	40	10.0	4	84	128	27	.80	85.9
DRIVE-IN DIFF.	140	125	.0	55	964	860	0	.96	99.8
SILICON NITRIDE	140	125	.0	60	964	860	0	.88	99.2
PLASMA PATTERN	10	40	.0	31	175	1115	0	.90	97.0
PLATING ETCH	1	450	3.0	8	8	3348	22	.93	96.4
IMMERSION PD A	1	500	3.0	8	11	3720	22	.93	96.2
SPIN DRY	1	0	.0	34	19	0	0	.96	98.5
SINTER 1	15	100	.0	2	28	191	0	.96	55.7
IMMERSION PD B	1	500	3.0	8	11	3720	22	.93	95.7
ELECTROLESS PD	1	500	3.0	8	11	3720	22	.93	95.5
SPIN DRY	1	0	.0	34	19	0	0	.96	97.3
SINTER 1	15	100	.0	2	28	191	0	.96	55.0
ELECTROLESS NI	1	500	3.0	11	16	5115	30	.93	91.6
SPIN DRY	1	0	.0	33	19	0	0	.96	99.3
SOLDER	15	4000	10.0	7	50	24639	54	.88	89.1
CELL TEST	2	0	.0	19	21	0	0	.95	95.6
CELL ATTACH	11	400	.0	19	115	6687	0	.88	97.8
MODULE CLEAN	1	400	10.0	9	4	3167	79	.88	99.9
MODULE ASSEMBLY	4	400	.0	9	19	3167	0	.88	99.8
RIVET-WELD	2	0	.0	3	3	0	0	.88	74.8
CURE	10	200	.0	11	60	2134	0	.97	92.5
MODULE TEST	2	0	.0	1	0	0	0	.95	51.9
TOTAL					3298	83888	455		

VENT CFM	=	Exhaust in cubic feet per minute for the process step
WTR GPM	=	Deionized water in gallons per minute for the process step
MACH EFF	=	Machine efficiency
EQPT UTL %	=	Equipment utilization %

Total Expense and Material Calculations

Utilizing data assumed and calculated previously, expense items for the individual process steps and process sequence can now be calculated.

Table 16 illustrates total incurred expenses, which include process expenses, electrical expenses, and DIH_2O expenses. Also presented in Table 16 are the total material cost items. Process expenses are the sum of all expendable items used in the manufacturing of solar cells. These items include, for example, chemicals, and are calculated by determining the cost per 1000 wafers produced multiplied by the number of wafers processed in a particular process step per hour and the number of production hours in a year (5400). Wasted silicon is included in this category. Also included in this category are items which are dependent on the number of machines used as well as items which depend on the number of machines used factored by that machine's efficiency and utility factor. Electrical expense is the product of the total electrical power (as defined in Section 3.6.2.7), 8766 annual hours, and a variable power rate which is nominally 2½¢/KWH. DIH_2O expense is the product of deionized water consumed per year times $.0031/gallon. Material items are calculated on a per 1000 wafer basis as well as a variable initial silicon cost figure.

TABLE 16

PHASE II PROCESS — 12CM CELL CONFIGURATION
100.0 MEGA WATT ANNUAL PRODUCTION — 14.00 % CELL EFFICIENCY
SOLAR CONCENTRATION = 1 SOLAR CONSTANTS
SILICON = $11.70/KILOGRAM — POWER RATE = 2.5 CENTS/KWH

EXPENSE & MATERIAL ITEMS

PROCESS STEP	PROCESS EXP(K$)	ELECT EXP(K$)	WATER EXP(K$)	TOTAL EXP(K$)	MATL (K$)
PLASMA ETCH	976.1	3.8	.0	979.9	.0
WAX APPLY	4.4	29.0	.0	33.4	.0
TEXTURE ETCH	84.4	14.2	.0	98.7	.0
WAX REMOVE	.0	9.8	45.8	55.6	.0
PLASMA CLEAN	9.6	3.7	.0	13.3	.0
ION IMPL-ADV P	14.1	48.4	129.0	191.5	.0
ION IMPL-ADV N	25.2	10.4	27.6	63.2	.0
DRIVE-IN DIFF.	48.5	117.4	.0	165.9	.0
SILICON NITRIDE	107.4	117.4	.0	224.8	.0
PLASMA PATTERN	18.1	22.7	.0	40.8	.0
PLATING ETCH	25.6	5.7	22.4	53.8	.0
IMMERSION PD A	2.1	6.7	22.4	31.2	27.8
SPIN DRY	.0	2.4	.0	2.4	.0
SINTER 1	3.8	3.7	.0	7.5	.0
IMMERSION PD B	2.1	6.7	22.4	31.2	3.5
ELECTROLESS PD	64.9	6.7	22.4	94.0	434.7
SPIN DRY	.0	2.4	.0	2.4	.0
SINTER 1	3.8	3.7	.0	7.5	.0
ELECTROLESS NI	.0	9.2	30.8	40.0	11.9
SPIN DRY	.0	2.3	.0	2.3	.0
SOLDER	412.9	41.0	55.2	509.0	459.3
CELL TEST	.0	2.6	.0	2.6	.0
CELL ATTACH	.0	23.4	.0	23.4	.0
MODULE CLEAN	.0	5.1	79.4	84.5	.0
MODULE ASSEMBLY	.0	6.8	.0	6.8	.0
RIVET-WELD	.0	.4	.0	.4	.0
CURE	.0	10.4	.0	10.4	.0
MODULE TEST	.0	.1	.0	.1	21952.3
TOTAL	1802.9	516.3	457.5	2776.7	22889.5

The key for Table 16 is:

PROCESS EXP (K$)	=	Process expenses in 1000 dollar units
ELECT EXP (K$)	=	Electrical power expenses in 1000 dollar units
WATER EXP (K$)	=	Deionized water expenses in 1000 dollar units
TOTAL EXP (K$)	=	Total expenses in 1000 dollar units
MATL (K$)	=	Material costs in 1000 dollar units

3.8.4 RESULTS

A summary of the total costs for the life of the factory is shown in Table 17. This table shows contributions of the cost categories of materials, expenses, labor, overhead, interest, and depreciation. For technology and automation levels equivalent to those existing today, the total value added to the starting substrate amounts to 0.4024/watt in 1975 dollars. Due to the assumptions made in the analysis, this can be considered as the upper limit of the value added cost for this process.

For the analyzed process sequence, significant portions of the total cost are associated with module assembly. A comparison of the relative costs and cost factors for cell processing and module assembly is shown in Table 18.

Module materials, it can be observed, are a major cost factor. The materials category contributes 49.8% of the total value added cost. Further, the module materials represent 96% of this, or nearly 48% of the total value added. This is an obvious candidate for cost reductions.

TABLE 17

Cost factors as a function of the phases of factory life. Phase I is the building phase, Phase 2 is the equipment phase, Phase 3 is the labor build-up phase, and Phase 4 is the production phase.

PHASE II PROCESS — 12CM CELL CONFIGURATION
100.0 MEGA WATT ANNUAL PRODUCTION — 14.00 % CELL EFFICIENCY
SOLAR CONCENTRATION = 1 SOLAR CONSTANTS
SILICON = $11.70/KILOGRAM — POWER RATE = 2.5 CENTS/KWH
DIRECT LABOR CENSUS = 822 — INTEREST RATE = 10.0 %

SUMMARY (K$)

FACTORY LIFE		MAT	EXP	LAB	OVP	INT	DEP	TOTAL
PHASE 1	6 MO	0	0	0	166	157	0	323
PHASE 2	6 MO	0	26	0	839	691	65	1621
PHASE 3	6 MO	5722	694	3033	2882	1441	1246	15019
PHASE 4	60 MO	114447	13884	45415	29754	8386	12459	224344
TOTAL COST		120170	14604	48448	33642	10675	13769	241308
TOTAL	$/WATT	.2345	.0285	.0945	.0656	.0208	.0269	.4708
%		49.8	6.1	20.1	13.9	4.4	5.7	100.0

INFLATION FACTOR 1.17
COST IN 1975 DOLLARS = $0.4024/WATT

	CELL		MODULE		
	Actual	(%) of Category Total	Actual	(%) of Category Total	Total
Capital Equip. (K$)	8568	69	3834	31	12402
Mfg. Floor Space (ft^2)	25869	56	20632	44	46501
Direct Labor/Shift	202	74	72	26	274
Electrical Power (KW)	3075	93	222	7	3298
Exhaust (CFM)	68733	82	15155	18	83888
Process Exp (K$)	1803	100	---	---	1803
Electrical Exp (K$)	467	91	49	9	516
Water Exp (K$)	379	83	79	17	458
Total Exp (K$)	2649	95	128	5	2777
Materials (K$)	938	4	21952	96	22890

TABLE 18: COMPARISON OF RELATIVE COSTS BETWEEN CELL FABRICATION AND MODULE ASSEMBLY FOR COST FACTORS AND CATEGORIES.

The second largest cost category contribution is labor, accounting for 20.1% of the total value-added. Automation will obviously reduce this contribution. Further, automation can effect some process simplifications, further reducing total costs through decreased expenses.

Cost savings can be envisioned in all other categories as well. For example, by utilizing a recirculating DI water system, consumed DI expenses can be reduced.

Other significant cost reductions can be achieved through process simplification. Combining ion implant activation anneal and silicon nitride deposition, and eliminating electroless palladium plating and attendant steps (both of which appear feasible) could save on the order of 2.5¢/watt and increase process yield simultaneously.

Achieving the 1986 goals, thus, appears entirely reasonable, utilizing the process sequence presented and incorporating improvements (and simplifications) that are now recognized and which present no requirement for technological breakthrough.

3.8.5 MODULE FABRICATION ECONOMICS

The cost analysis indicates that interconnect and module designs incorporated in the process sequence being currently developed may be expensive relative to a 50¢/watt objective. Further analysis of this module design, relative to the future use of large square or rectangular solar cells, indicates that it can, indeed be sufficiently cost effective for incorporation in a 50¢/watt product.

There is a logical breaking of the overall process sequence into three separate areas: silicon substrate production, cell fabrication, and encapsulation (including interconnect). The current program has emphasized almost exclusively cell fabrication into water substrates with the added proviso that the process seqeunce be easily applicable to ribbon substrates. This program was intended to provide an important step leading to the economical production of high efficiency solar cells. These cells, in theory, could be incorporated into virtually any module design, varying from the high degree of protection afforded by the Motorola module to the more limited cell protection offered by some other designs.

The stated goal of a 20 year module life should be considered a minimum goal, not a goal to be missed or achieved marginally. The impact of module life on system economics is large. Module reliability is perhaps the single most important cost factor in module design. Unfortunately, in the absence of either 20 year test data or proven accelerated life testing figures, it is not possible to quantitatively predict whether a given module design will achieve the desired 20 year life. Accordingly, module designs proposed strictly on the basis of cost will probably not meet the requirement of a 20 year life. At the present time, evaluation of the long term reliability of a given module design must rely heavily on prior history of the semiconductor industry, utilizing what data are available from the (recent) solar module industry, and engineering common sense.

Broad experience in failure analysis by the semiconductor industry has resulted in the observation that, passing initial screening tests, one of the most likely long-term catastrophic failure modes in solar cell modules will be associated with cell metallization and metal interconnection. (Also likely will be mechanical failures such as cell breakage, and module component delamination.) The module, ideally, should be capable of protecting the

metallization and interconnects while, at the same time, be capable of cushioning the cells mechanically.

The module design proposal by Motorola was chosen because, on the basis of reliability of the materials and engineering judgement of the design, it appears truly capable of meeting a 20 year minimum life. The high cost, in terms of a 50¢/watt module, is due in large part to the high present cost of the copper-kapton cell interconnect sheet. This interconnect sheet is presently utilized in the Motorola product line for round solar cells.

In order to meet future (1986 and beyond) cost goals, module efficiency requirements will demand a high cell efficiency and packing factor. This will amost certainly be met by square or rectangular cells. Such rectangular cells may be easily interconnected in sich a fashion that the copper-kapton laminate will be unnecessary. This will remove a major cost item from the module materials. Can the remaining materials meet $.50/watt cost goals? It appears so.

For the sake of discussion, let us assume that the $0.50/watt can be very stringently allocated as:

$0.13 Silicon Substrate

$0.13 Cell Fabrication

$0.13 Encapsulation

$0.11 Profit

If one area costs somewhat more, profit is reduced. Further assume that the module efficiency is 15%, a goal many manufacturers have publicly noted as feasible. This means that, at 100 watts/ft^2 insolation, encapsulation can cost up to ($0.13)(15%)(100 watts/ft^2) or $1.95/ft^2. Looking at material costs for glass, steel, potting, frames, feed-throughs, etc., total costs of less than $1.50/ft.^{2} are readily achieved for several permutations of thicknesses for various structural designs; leaving nearly $0.50/ft^2 for labor, depreciation, etc.

This synergystic encapsulation concept -- a stable metallization (and interconnection) system in an effective package -- is expected to demonstrate a module life of appreciably more than 20 years while still being capable of inclusion in a 50¢/watt product. If an absolutely stable metallization-interconnect system is evolved, then the package may be cheapened; if an absolutely stable package is found, the metallization and interconnect can be further reduced in cost.

Until such time that reliability can be assured for 20 years with minimal encapsulation, evaluation of module designs and cost reduction modifications must continue. This will be a dynamic process and will, hopefully, result in a major reduction in the stringent requirements now identified being necessary for assuring reliability.

3.9 VERIFICATION OF PERFORMANCE

Verification (control) points have been defined for each process step and for the process sequence. In general, the process sequence can be considered successful only if a high yield is obtained at the module level. Testing of cells going into the modules and testing of completed modules, thus, are two key control points. Other key control points are utilized for evaluation of cells in-process, and must be related to final cell performance.

Control points should be incorporated into the process sequence, at least on a sampling basis, sufficient to guarantee that rapid, unambiguous identification of a processing problem can be made. The interpretive feature of such trouble-shooting is of key importance. Sufficient data should be compiled during processing to make an unambiguous analysis. For example, it is necessary to distinguish whether a poor cell fill factor is the result of a defective p-n junction, contamination by a lifetime killer, high sheet resistance

of the upper P-N junction region, inadequate metal, metal ingression to the vicinity of the p-n junction, or metallization of exposed areas of the p-n junction as a result of etched or broken textured peaks.

3.9.1 VERIFICATION OF PLASMA ETCHING

3.9.1.1 PLASMA SILICON ETCHING

Verification of satisfactory process control for plasma silicon etching is indirect and requires a time-lag between process performance and process verification. Following etching, completeness of damage removal can be verified by selective etch-pit techniques, or by analytical techniques such as X-ray topography. Etch-pit counting is limited to observing major amounts of residual damage; since it also etches the silicon, it can remove small amounts of residual damage. The process controls should, ideally, provide for a minimum amount of undamaged silicon being removed while still ensuring complete removal of the damaged layer. Accurate knowledge and control of the amount of damage created by a particular sawing technique is critical to economical operation of the sawing process. For example, if insufficient material is removed, final cell performance will be degraded. On the other hand, if too much material is removed, the process expends more time than necessary, consumes more materials, etc. Routine analysis of the depth of saw damage is, thus, a necessary control point.

3.9.1.2 PLASMA SILICON NITRIDE ETCHING

Process verification of silicon nitride patterning is accomplished primarily by visual inspection, utilizing both optical microscopy and scanning electron microscopy (SEM). In addition to inspection for completeness of removal, inspection must also be made for silicon etching and for nitride removal in

undesired areas. The latter is, of course, dependent upon the quality of masking. The other key parameter is pattern line width, which is also verified by visual inspection.

3.9.2 VERIFICATION OF WAX MASKING

Verification of the quality of the wax masking again relies upon visual criteria. Control inspection may be readily performed both after application and after etching. Both are capable of being done in-line by automatic equipment.

3.9.3 ION IMPLANTATION PERFORMANCE

In addition to in-process monitoring of the implant dose and voltage, control of ion implantation parameters relies upon measurement of substrates after activation anneal. The most rapid turn-around of information can be achieved through sheet resistance and photoresponse measurements, either on a continuous basis or through selective sampling.

3.9.4 PROCESS SEQUENCE VERIFICATION

Proof of total cell process sequence performance can be evaluated meaningfully only through electrical testing of completed solar cells, and subsequent measurement of interconnected and encapsulated cells. Here, visual inspection is also useful in identifying potential reliability problems.

3.9.5 SOLAR CELL AND MODULE FABRICATION

As verification of performance of the process sequence, Motorola has fabricated and delivered 500 cells and the modules (incorporating 96 of the cells) to JPL.

4.0 CONCLUSIONS

The work performed during this contract allows numerous conclusions to be drawn with respect to individual process steps and the overall process sequence developed.

Wax masking of texture etching can be achieved by either of two methods. Application and removal may be performed with a wax-solvent system. Alternatively, a melted wax technology has been shown to be practical and to offer significant cost and environmental advantages over the use of wax-solvent systems.

Plasma technology has been demonstrated to be practical for both solution etching and patterning of silicon nitride. Taken from an essentially untried state at the beginning of this contract, mechanically masked patterning of silicon nitride has progressed far beyond feasibility demonstration. Further studies are imperative, however, to establish requisite control parameters for true technology readiness.

Reduced pressure chemical vapor deposition of silicon nitride has been documented as a cost-effective, production ready technology.

Ion implantation studies have shown that this technology is capable of producing high efficiency solar cells. Photoresponse data from test wafers indicate that implant dose for optimum solar cell performance fall within the approximate range of 3×10^{14} cm^{-2} to 3×10^{15} cm^{-2} for phosphorus, arsenic, and boron dopant implants. Optimum cost-effectiveness is indicated at low implant energies. Activation annealing experiments have shown that simple moderate temperature cycles are at least equivalent to more complex multi-temperature cycles. The complex interactions between dopant species, implant energy, implant dose, and activation anneal cycle are not completely understood at this time. Studies are continuing in this area to establish technology readiness.

A viable cost-effective metallization system has been developed under separate contract and incorporated into this process sequence. Process simplifications have been shown to be feasible, making this system more cost-effective.

Smaller textured peak size has been shown to have a synergistic effect on improving the process sequence. Control of textured surface peak size can be obtained by simple bath parameters (composition and temperature) without need to employ more complicated mechanical techniques to obtain small, uniform peaks.

A detailed cost analysis for the Phase II process sequence has been performed for comparison with the Phase I cost study. An essentially upper-limit cost of value added to the starting substrate for the process being developed has been shown to be near $0.40/watt (in 1975 dollars). This process sequence cost includes both cell processing and module assembly. The module assembly incorporates stringent encapsulation requirements consistant with materials of known reliability. Reduced encapsulation requirements and automation are obvious candidates for cost reductions, and should be able to bring costs down to a level compatible with a complete module cost of less than $0.50/watt.

5.0 RECOMMENDATIONS

There is need for additional effort on specific process steps to bring the total process sequence to the point of production readiness. Increased emphasis should be placed on ion implantation and activation annealing technology in order to optimize the interactive parameters of implant species, implant energy and dose, and activation anneal cycle. These studies include combination of the activation anneal with the low pressure chemical vapor deposition of silicon nitride. Further, emphasis should remain high on the mechanically masked patterning of silicon nitride in a plasma in order to establish an increased understanding of the process so that the most cost-effective control ranges on important parameters may be defined. In all cases, the effects of process step modifications on the performance of the overall process sequence must be ascertained.

6.0 CURRENT PROBLEMS

There are no current problems which remain unsolved.

7.0 WORK PLAN STATUS

The work plan is complete.

8.0 LIST OF ACTION ITEMS

No items requiring unusual action exist for this contract.